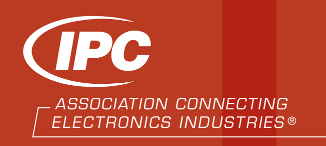
IPC-7095A

Design and Assembly Process Implementation for BGAs

October 2004



3000 Lakeside Drive, Suite 309S, Bannockburn, IL, 60015-1249
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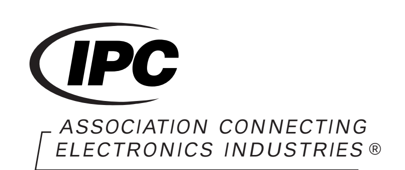
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Users of this publication are encouraged to participate in the development of future revisions.

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Table of Contents

Figures

Tables

Design and Assembly Process Implementation for BGAs

1 SCOPE

This document describes the design and assembly challenges for implementing Ball Grid Array (BGA) and Fine Pitch BGA (FBGA) technology. The effect of BGA and FBGA on current technology and component types is also addressed. The focus on the information contained herein is on critical inspection, repair, and reliability issues associated with BGAs.

1.1 Purpose The target audiences for this document are managers, design and process engineers, and operators and technicians who deal with the electronic assembly, inspection, and repair processes. The intent is to provide useful and practical information to those who are using BGAs and those who are considering BGA implementation.

1.2 Selection Criteria (Determination of Package Style and Assembly Processes) Every electronic system consists of various parts: interfaces, electronic storage media, and the printed board assembly. Typically, the complexity of these systems is reflected in both the type of components used and their interconnecting structure. The more complex the components, as judged by the amount of input/output terminals they possess, the more complex is the interconnecting substrate.

Cost and performance drivers have resulted in increased component density, and a greater number of components attached to a single assembly, while the available mounting real estate has shrunk. In addition, the number of functions per device has increased and this is accommodated by using increased I/O count and reduced contact pitch. Reduced contact pitch represents challenges for both assemblers and bare board manufacturers. Assemblers encounter handling, coplanarity and alignment problems.

The board manufacturers must deal with land size issues, solder mask resolution and electrical test problems.

Based on industry predictions one would believe that all component packages have over 200 I/Os and are increasing in I/O count. Actually, components with the highest usage have I/O counts in the 16 to 64 I/O range. Over 50% of all components fall into this category, while only 5% of all components used have over 208 I/Os, which may be the threshold for determining the cross-over point between peripheral leaded component style packages and array type formats.

Many peripherally leaded, lower I/O count devices, such as memory and logic devices, are being converted to area array packaging formats as either BGAs or Fine Pitch BGAs.

Although the percentage of high I/O components used on an electronic assembly is small, they play a big part in driving the industry infrastructure for both bare board and assembly manufacturing. These high I/O components determine the process for bare board imaging, etching, testing and surface finishing. They determine the materials used for fabrication and drive assembly process improvements in a similar manner.

The electronics industry has evolved from using through-hole assembly technology in which the component leads went into the printed board substrate and were either soldered to the bottom side of the board or into a plated-through hole. Surface Mounting Technology (SMT) has advanced to a stage where the majority of electronic components manufactured today are only available in SMT form.

Manufacturing products with SMT in any significant volume requires automation. For low volume, a manually operated machine or a single placement machine may be sufficient. High volume SMT manufacturing requires special solder paste deposition systems, multiple and various placement machines, in-line solder reflow systems and cleaning systems.

The heart of surface mount manufacturing is the machine that places the components onto the printed board land areas prior to soldering. Unlike through-hole (TH) insertion machines, surface mount placement machines are usually capable of placing many different component types. As design densities have increased, new SMT package styles have evolved. Examples are Fine Pitch Technology (FPT), Ultra Fine Pitch Technology (UFPT), and Array Surface Mount (ASM). This latter category consists of the many families of ball or column grid arrays and the chip scale packages (CSP) and Fine Pitch BGAs (FBGA). These parts are all capable of being placed by machines provided that the equipment has the required positioning accuracy.

Increased device complexity has been a primary driving factor for SMT. In order to minimize the component package size, component lead spacing has decreased (e.g., 1.27 mm to 0.65 mm). Further increases in semiconductor integration requiring more than 196 I/Os can drive packages to even closer perimeter lead spacing, such as 0.5 mm, 0.4 mm, 0.3 mm, and 0.25 mm. However, the array package format has become the favorite for high I/O count devices. Area array component package styles have a pitch that originally was much larger than the equivalent peripherally leaded device, however that lead format is now also seeing reductions in pitch configurations.

Ball and column grid arrays were standardized in 1992 with 1.5, 1.27 and 1.0 mm pitch. Fine Pitch BGA array packages standards have established pitches of 1.0 mm, 0.8, 0.75, 0.65, and 0.5 mm. There are some implementations of FBGAs where the pitch has been reduced to 0.4 mm, and future components are being evaluated with 0.3 and 0.25 mm pitch configurations.

The via pattern for the board requires much tighter feature control as the pitch for BGA, FBGA and CSP becomes smaller. There is a question as to how many lead pitches are required between 1.0 mm and 0.5 mm. Some indicate that a 60% rule is of value where the ball diameter is 60% of the pitch. This results in a 0.5 mm ball diameter for a 0.8 mm pitch. FBGA would use a 0.4 mm ball diameter for a 0.65 mm pitch. On the other hand, some feel that it would be better to standardize a 0.3 mm diameter ball for all FBGA packages.

Standardization of a single ball size would facilitate many characteristics. The motive is to accommodate conductor routing on the interconnecting substrate and help standardize socket pin contact design.

Area array packaging has the intrinsic value of being able to make coherent designs. This is exemplified on the right side of Figure 1-1, where a single pitch might be depopulated to meet the requirements of the design. The trend illustrated on the left side of Figure 1-1 forces the creation of many different test sockets. Interconnection of the part IOs is affected both by ball pitch and ball diameter. The standard ball diameter as specified by the US JEDEC JC11 Committee alleviates pressure on the substrate design.

The selection process for an electronic assembly should attempt to minimize the variation in component package types and the I/O pitch condition. The large I/O count devices and problems with assembly of finer pitch peripheral packages has caused rethinking of the packaging style vs. the assembly complexity relationship, and the printed board interconnection and surface characteristics.

The concern in using these very complex parts relates to board design and assembly issues. Assembly is concerned about attaching all the leads to the mounting structure without bridging (shorts) or missing solder joints (opens). Design is concerned with interconnecting all the leads and having sufficient room for routing conductors.

Array packages permit a variety of ball configurations, e.g., staggered positions or partially populated parts, to provide the room required for adequate conductor routing. With a common base array pitch significant advantages can be gained in terms of providing a coherent standard for all of the elements of the electronic manufacturing infrastructure for components, sockets, substrates and test systems (see Figure 1-2).

The role of the interconnecting substrate continues to grow performing circuit functions beyond simply providing interconnection wiring. In addition, organic copper clad laminates have been targeted to replace the ceramic interconnecting structure inside large components, such as Plastic Ball Grid Arrays (BGAs) or Array formatted SMDs as shown in Figure 1-3. Thus organic substrates must meet the thermal and moisture-resistance profile for the single chip or multi device BGA configuration parts, as well as the performance requirements defined by the present standards.

The interconnecting and mounting structure will require greater precision in the placement and definition of the conductors and in the dielectric properties of the material.

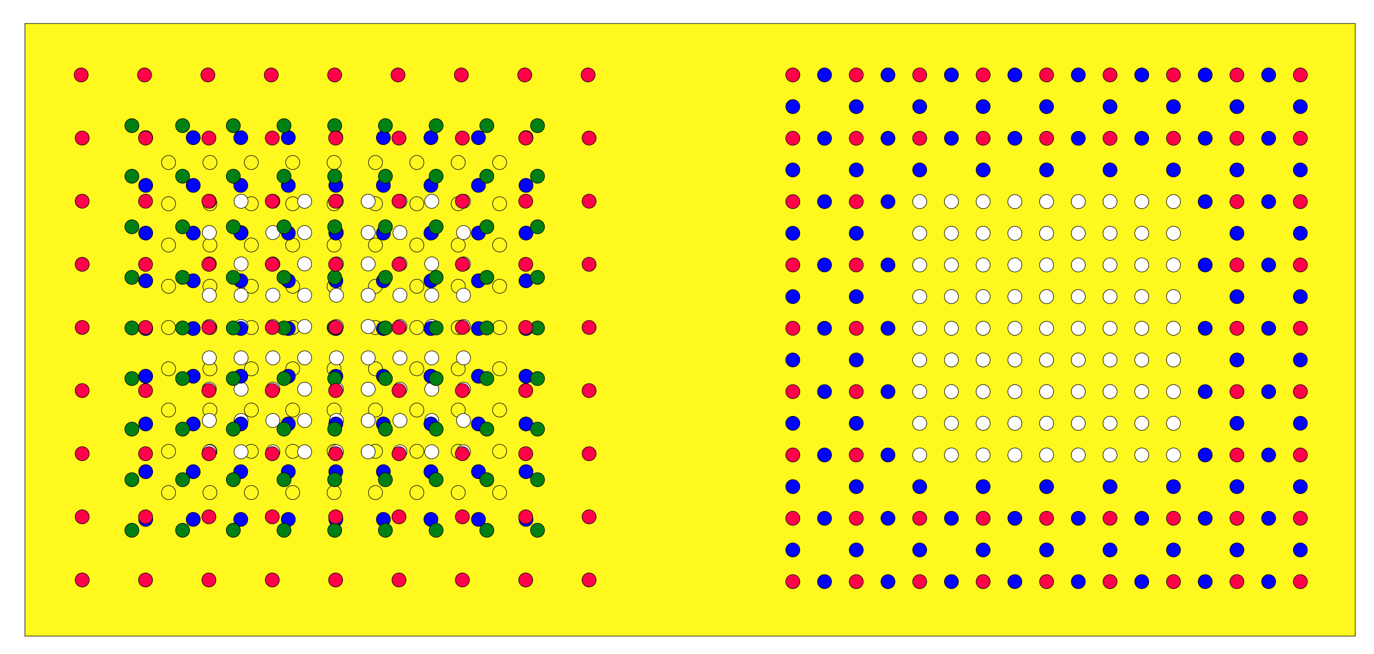


Figure 1-1 Area Array I/O Position Comparisons

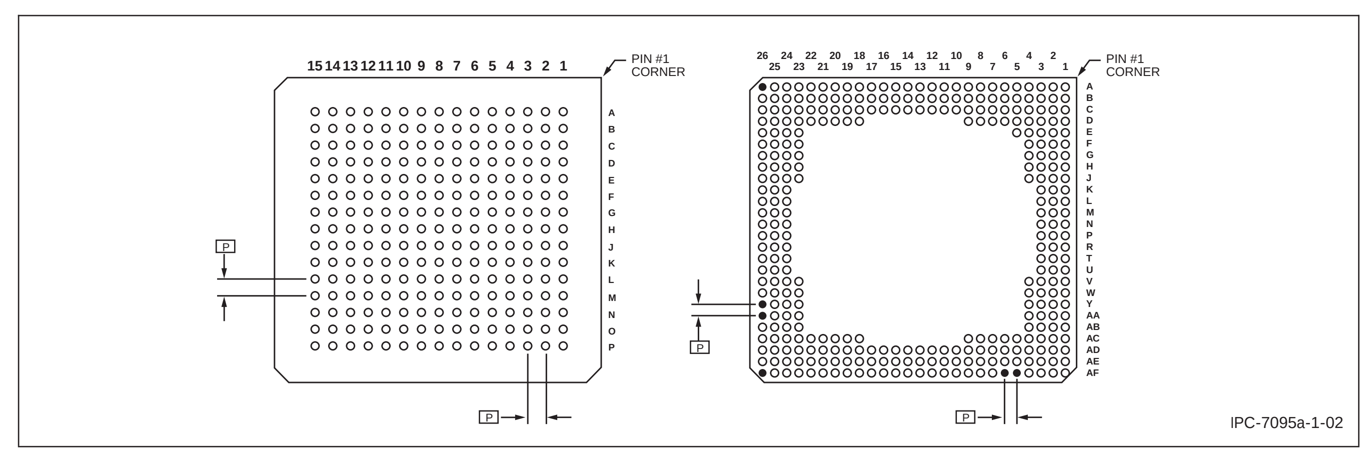


Figure 1-2 Area Array I/O Position Patterns

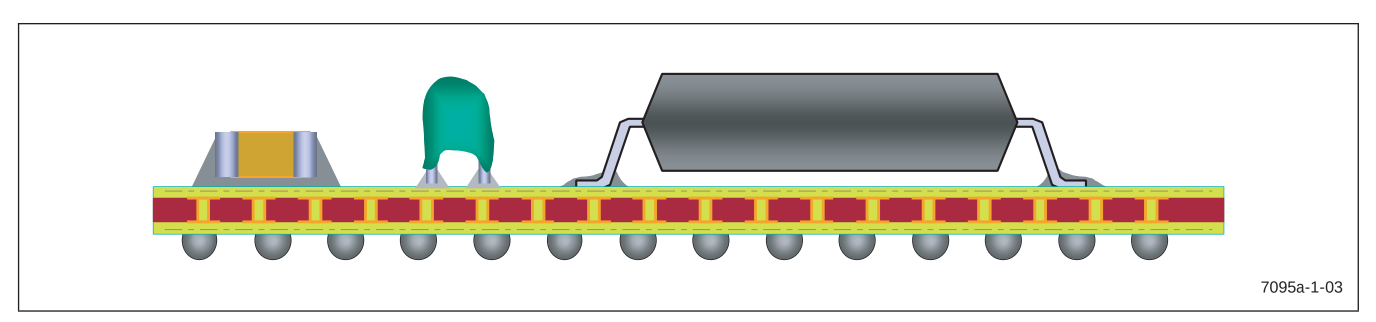


Figure 1-3 Application Specific Module (ASM) Ball Grid Array Format

Moreover, the substrate used will likely require that the interconnecting structure already contain materials necessary for attachment of the components (e.g., solder bumps, palladium coated lands, conductive adhesive).

With more of the circuit customization going into silicon and with the component package size increasing, the printed board design will need to change. The higher I/O demand will require multilayer or high-density interconnection (microvia) designs to support the required wiring and to provide escape routing from the internal connections of array component patterns to the printed board. Both sides of the printed board may be required to place all the components required by the design. There will also be an increased demand on the printed board to handle the required power dissipation.

Using high I/O components like BGAs and fine pitch BGAs creates the challenge of routing all the required signal, power, and ground I/O balls to the PWB without increasing PWB complexity and therefore cost. Thoughtful package pin assignments and the package configuration considerations (pitch, ball size, ball count, and depopulation) can go a long way in making the board routing easier.

Two interconnection signal layers can be sufficient for BGA package escape, even when the BGA has very high ball counts, providing the pin assignments are properly planned and the escape routing is carefully designed. Table 1-1 indicates the number of ''escapes'' possible on two layers of circuitry versus the array size and the number of conductors between lands/vias. It should be noted that as the number of I/O increases, the ability to escape diminishes and thus more layers may be required. At first glance, Table 1-1 might appear to indicate that two routing layers are insufficient to escape any array greater than 16 x 16 (256 balls). In reality, a significant number of the balls will be used for power and ground connections and therefore do not need ''escape'' routing. They can be directly connected to the appropriate plane through the dogbone via attached to the land. That being said, poor placement of the signal or power/ground balls can ''waste'' available routing channels and significantly reduce the total number of signal I/Os that can be routed out in a given number of layers.

Table 1-1 Number of Escapes Vs. Array Size on Two Layers of Circuitry

<table>
<tr><th rowspan="3">Array Size</th><th rowspan="3">Total Leads</th><th colspan="3">Number of Conductors Between Vias (•|•)</th></tr>
<tr><th>1</th><th>2</th><th>3</th></tr>
<tr><th>•|•</th><th>•||•</th><th>•|||•</th></tr>
<tr><td>14 X 14</td><td>196</td><td>192</td><td>196</td><td>196</td></tr>
<tr><td>16 X 16</td><td>256</td><td>236</td><td>256</td><td>256</td></tr>
<tr><td>19 X 19</td><td>361</td><td>272</td><td>316</td><td>352</td></tr>
<tr><td>21 X 21</td><td>441</td><td>304</td><td>356</td><td>400</td></tr>
<tr><td>25 X 25</td><td>625</td><td>368</td><td>436</td><td>496</td></tr>
<tr><td>31 X 31</td><td>961</td><td>464</td><td>556</td><td>640</td></tr>
<tr><td>35 X 35</td><td>1225</td><td>528</td><td>638</td><td>736</td></tr>
</table>

Placing signal pin assignments on the outer rows of an array package, and using the inner balls for power and ground will facilitate escape routing. However, the corner balls of large array packages are more suspectible to mechanical failure, and therefore it may be better to use these for redundant ground connections.The number of rows of signal I/O that can be routed out will depend on the desired number of conductor routing layers in the printed board and the number of conductors that can be routed between lands and vias.

Figure 1-4 shows examples of conductor and space widths that will fit between adjacent lands with various pitches and land diameters. Note that as the ball pitch decreases, the conductor width and spacing for a given number of conductors per channel also decreases, and it becomes more difficult and costly to produce the board. Using 150 µm conductors and spaces is quite cost effective, but printed board cost begins to increase significantly for 100 µm conductors and spaces.

Using an organic interconnecting substrate to mount the bare die within a plastic BGA requires that the mounting lands on the substrate match the bonding lands on the die.

The bonding lands are typically positioned for wire bonding, since this is the most popular technique. Thermally conductive adhesive is one of the methods used to attach the back of the die to the substrate. Depending on the number of I/O and the lead pitch, multilayer substrate fabrication techniques may be used to translate a peripheral bonding land die, to an area array matrix of bumps, balls, or columns (see Figure 1-5).

The transition of chip bonding lands that are in an array format permits the mounting of the die in flip chip configurations. In this instance, the die is mounted opposite to that which is wire-bonded and the bumps of the die come into direct contact with the substrate being used to convert the die pattern to the BGA pattern. This creates new challenges for the routing requirements for the organic high-density microcircuit board manufacturer. In addition, underfill is usually required to maintain some consistency between the CTE of the chip and the CTE of the organic multilayer board (see Figure 1-6).

To accommodate a flip chip with area array I/O lands at 0.25 mm pitch, the BGA package substrate will need bonding lands at 0.25 mm pitch on the top side, and solder balls at 1.27 or 1.00 mm pitch on the bottom side. These opposing sets of lands must be connected by the BGA package substrate (High-Density Microcircuit Board) wiring and interlevel vias or PTHs. It may be necessary to have one or more interconnecting lines between two adjacent bonding lands on the topside of the BGA substrate. This is done in order to access multiple rows of the interior I/O lands for connection to the vias or PTHs for eventual connection to the solder balls on the bottom side. Very aggressive layout rules must be used, even when designing with surface redistribution layers (see Figure 1-7).

For high performance chips with 1700 pin requirements, a BGA with very dense wiring layers is required. The body size of such a BGA would be 50 mm. In all probability, there would be depopulated solder balls in the middle of the BGA. Regarding pitch, such a BGA substrate would require a 1.00 mm via and solder ball pitch, which would accommodate a ball density of 100 I/O per square centimeter.

1.2.1 Technology Comparison The principles used to mount a single chip into an organic carrier package can also be used to connect several chips together. This technique is referred to as a multichip module-laminate (MCM-L) or a multichip package (MCP) or the new name assigned to complex module assemblies known as multi Device Subassembly (MDS). In all the variations that are being developed the one governing condition is the use of the area array format. Thus, ball size and pitch will continue to be the process governing factor for individual components or those that encompass more than one semiconductor die. Table 1-2 shows some examples of an attempt to establish a definition for Multichip modules housing more than one die. Figure 1-8 is an example of one such product using the area array concepts for interconnection.

Possible other descriptive attributes include substrate technology (e.g., -C for ceramic, -L for laminate, -D for deposited, - W for wafer, -S for silicon) & interconnection technology (e.g., -WB for wire bond, -FC for flip chip, - MX for mixed).

Microprocessors typically have between 40 - 60% of their I/O dedicated to power and ground. As an example, a package might have a total of 1300 - 1400 I/O where the signal count is between 600 and 700 I/O. Applications Specific ICs (ASICs) may differ in that I/O apportionment. The signal I/O escape wiring, and their interconnection to other high I/O packages, will also require very high density printed boards (HDBs). As the number of I/O on a chip increases further, the body size of the single chip package may become unacceptably large, and could require reassessment of the overall package solution, including considering multichip module packaging or Application Specific Module Packaging as an alternative.

The signal I/O count for high performance BGAs is about 2.5 times that commonly required for BGAs used in hand held products. The interconnection density requirement is linearly proportional to the number of signal I/O per package, and inversely proportional to the center-to-center pitch between adjacent packages. A 2.5X increase in signal I/O from 500 to 1300 pins per package at the same package-to-package pitch will require a PWB with a 2.5X increase in its wiring density, and a proportional increase in the density of the interlevel vias or PTHs. This may require a

	0.25 mm Pitch	0.5 mm Pitch	0.75 mm Pitch	1.0 mm Pitch	1.27 mm Pitch
Conventional FR-4 125 µm Line 125 µm Space 700 µm Land					
Conventional FR-4 125 µm Line 125 µm Space 600 µm Land					
High Density FR-4 100 µm Line 100 µm Space 600 µm Land					
Next Gen FR-4 60 µm Line 50 µm Space 300 µm Land					
Typical Microvia 75 µm Line 100 µm Space 200 µm Land					
Next Gen Microvia 50 µm Line 50 µm Space 50 µm Land					

Figure 1-4 Conductor Width to Pitch Relationship

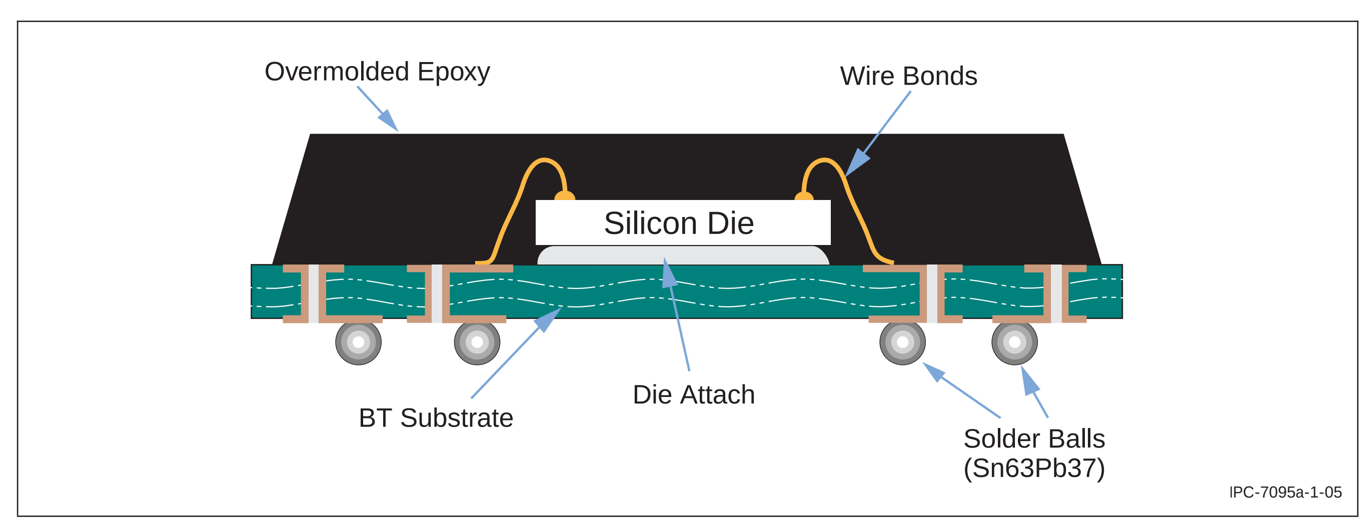


Figure 1-5 Plastic Ball Grid Array, Chip Wire Bonded

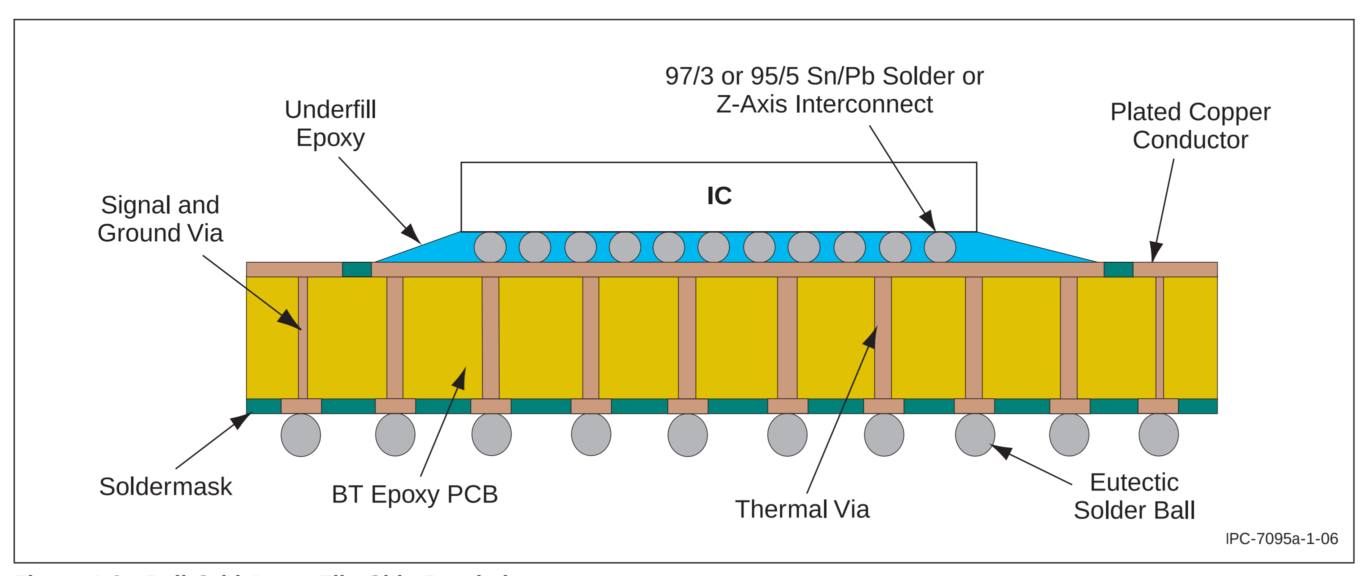


Figure 1-6 Ball Grid Array, Flip Chip Bonded

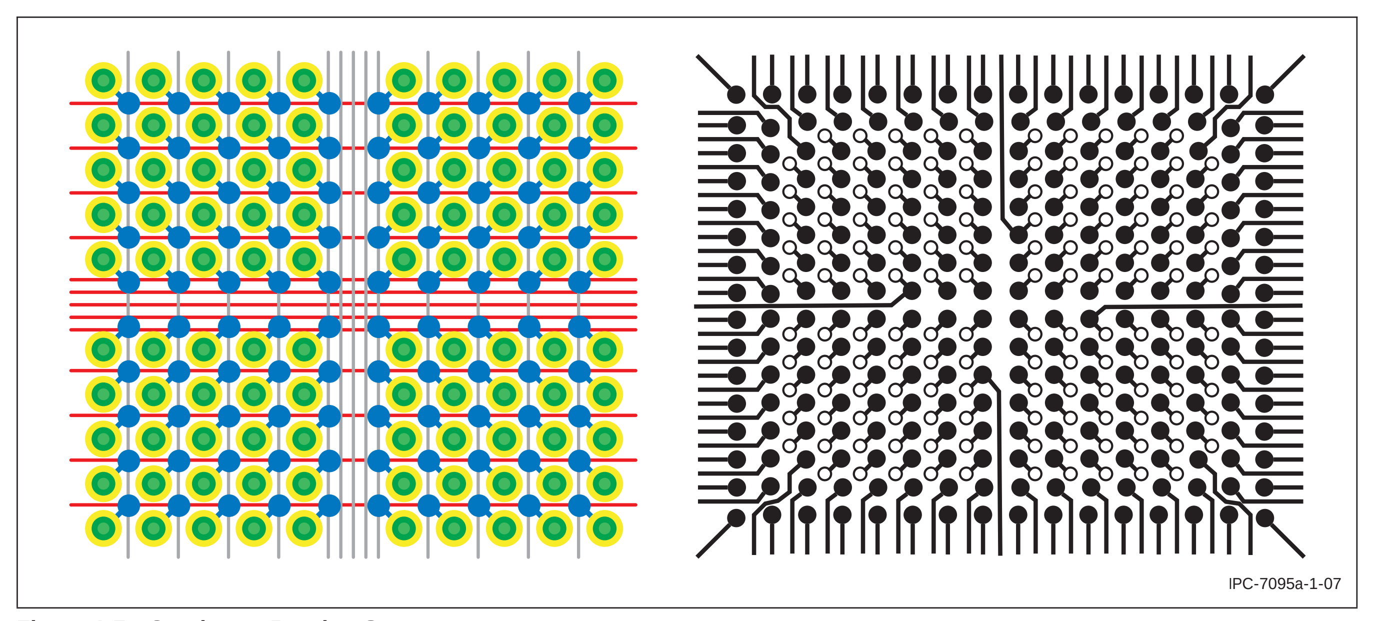


Figure 1-7 Conductor Routing Strategy

Table 1-2 Multichip Module Definitions

MCM	Technology Description	Attributes
Type 1	Common Technology Package	Multiple same type chips, in plane.
Type 1S	Common Technology Package	Multiple same type chips, stacked.
Type 1F	Common Technology Package	Multiple same type chips, folded.
Type 2	Mixed Technology Package	Mixed IC technology package, in plane.
Type 2S	Mixed Technology Package	Mixed IC technology package, stacked.
Type 2F	Mixed Technology Package	Mixed IC technology package, folded.
Type 3	System in Package	Mixed ICs and discrete devices, in plane.
Type 3S	System in Package	Mixed ICs and discrete devices, stacked.
Type 4	Optoelectronic System Package	Mixed technology for optoelectronics.

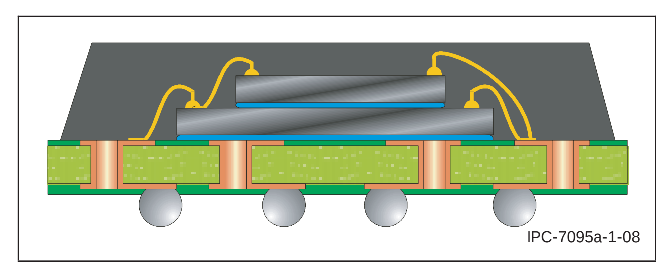


Figure 1-8 MCM Type 2S-L-WB

reduction in the PTH/via pitch, and an increase in the number of signal layers in the PWB.

2 APPLICABLE DOCUMENTS

2.1 IPC[1]

J-STD-013 Implementation of Ball Grid Array and other High Density Technology

J-STD-020 Handling Requirements for Moisture Sensitive Components

J-STD-029 Test Methods for Flip Chip or Chip Scale Products

J-STD-032 Performance Standard for Ball Grid Array Balls

J-STD-033 Standard for Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices

IPC-T-50 Terms and Definitions for Printed Boards and Printed Board Assemblies

IPC-D-279 Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies

IPC-D-325 Documentation Requirements for Printed Boards

IPC-D-350 Printed Board Description in Digital Form

IPC-D-356 Bare Substrate Electrical Test Information in Digital Form

IPC-SM-785 Guidelines for Accelerated Reliability Testing of Surface Mount Attachments

IPC-2221 Generic Standard on Printed Board Design

IPC-2225 Sectional Design Standard for Organic Multichip Modules (MCM-L) and MCM-L Assemblies

IPC-2226 Design Standard for High Density Array or Peripheral Leaded Component Mounting Structures

IPC-2511 Generic Requirements for Implementation of Product Manufacturing Description Data and Transfer

IPC-2581 Generic Requirements for Printed Board Assembly Products Manufacturing Description Data and Transfer Methodology

IPC-6011 Generic Performance Specification for Printed Boards

IPC-6015 Qualification and Performance Requirements for Organic Multichip Module (MCM-L) Mounting and Interconnecting Structures

IPC-6016 Qualification and Performance Specification for High Density Interconnect (HDI) Layers or Boards

IPC-7071 Generic Requirements for Component Mounting

IPC-7075 Sectional Requirements for High Pin Count Area Array Component Mounting

IPC-7076 Sectional Requirements for Chip Scale and Chip Size Component Mounting

IPC-7077 Sectional Requirements for Wire Bonding Bare Chip Component Mounting (Chip on Board)

IPC-7078 Sectional Requirements for Flip Chip Component Mounting (Direct Chip Attach)

IPC-9701 Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments

2.2 JEDEC[2]

Publication 95 Mechanical Outlines of Solid State and Related Products

Publication 95 Section 4 Design Requirements for BGA and FBGA

JESD22-A102B Accelerated Moisture Resistance - Unbiased Autoclave

3 MANAGING BGA IMPLEMENTATION

Component packaging in general, microprocessor and memory packages in particular, drive the rest of the electronic assembly packaging issues. The driving forces for component packaging are thermal and electrical performance, real estate constraints and cost. Peripheral devices with 1.27 mm pitch have become commonplace in the industry. However, this package cannot accommodate higher than 84 pins. Larger peripheral pin count devices require lead pitches of 0.65 mm, 0.5 mm or 0.3 mm.

1. www.ipc.org
2. www.jedec.org

Although pitches below 1.27 mm are useful for reducing package size, the increased density presents many problems for most manufacturers. At these fine-pitches, leads are very fragile and susceptible to damage such as lead coplanarity, lead bending and sweep. To place these packages, a pick-and-place machine with vision system and waffle pack handlers is necessary. These two features, however, can add substantial capital equipment costs.

The finer particle solder pastes needed for these fine-pitch packages tend to increase viscosity and lower print speed. Also, design guidelines must change to allow added inter-package spacing between the fine-pitch devices and neighboring conventional packages. With the exception of no-clean fluxes, cleaning problems arise with fine-pitch devices which sit almost flush (0 to 250 µm) to the board. For proper cleaning, a 0.4 mm to 0.5 mm standoff is required. Using a temporary solder mask over the vias under a package avoids flux entrapment problems. However, this extra process step increases production cost.

Since BGAs use solder bump interconnections instead of leads, problems associated with lead damage and coplanarity are eliminated. BGA pitches from 1.27 mm to 1.5 mm, have well over 250 µm of standoff height, so problems with paste printing, placement, reflow and cleaning are significantly reduced. BGAs also provide much shorter signal paths compared to fine-pitch devices. Shorter signal paths can be very critical in high-speed applications.

3.1 Description of Infrastructure The use of BGAs in the design through assembly processes has become common place in the last few years. Never-the-less incorporating these parts into electronic assemblies requires dedicated engineering resources to develop, implement and integrate the processes into the assembly operation. Even though BGA can leverage existing SMT infrastructure, there are many technical considerations that must be addressed in order to be successful in implementing BGA components into existing product configurations.

3.1.1 Land Patterns and Circuit Board Considerations Components are soldered to the printed board on the surface mount lands. Lands are areas of copper approximately the shape and size of the lead or termination footprint. The land pattern design is critical for manufacturability, because it affects the solder defect rate, cleanability, testability, repair/rework and the solder joint's reliability.

In the past, component tolerances were too liberal (some still are) for effectively designing land patterns. Additionally, since surface mount packages were not standardized, land pattern design could not be standardized. As a result, users had to develop in-house land pattern dimensions and qualify a limited number of suppliers who met those specifications. Reducing the number of suppliers reduced the range of sizes and associated tolerances required of land pattern design.

Land pattern design issues for BGA need to be understood. This is essential to assure proper solder joint formation and prevent defects such as bridging, opens and to achieve optimal reliability. In addition to land design, one should also keep in mind that the inner rows of BGA pins require additional layers for interconnection. Increasing the number of pins (vias) drives layer count due to the reduction of routing channels. Higher layer count means higher cost of the bare board.

BGA lands can be solder mask defined (solder mask overlaps the land) or copper defined (solder mask stays away from the land). There are pros and cons of each approach but the copper defined lands are more reliable.

3.1.2 Assembly Equipment Impact Getting into BGA technology also requires some new assembly capability. Depending upon the type of pick and place systems, a change in package carrier mechanism may also be required to transfer packages from matrix tray to the pick position. Fiducials may also be helpful in helping the vision systems recognize the exact location of the land pattern for the BGA, similar to what is used for fine-pitch peripheral leaded parts. Large BGA parts on tape-and-reel will require 44 mm and 56 mm feeders depending on the body size. Reflow will require use of a forced air convection oven. Repair and inspection of BGAs are rather difficult. Rework machines with paste deposition, preheat, and vision capability may not be required, but are very helpful. X-ray and optical inspection (endoscope) capability for process development is a benefit.

3.1.3 Stencil Requirements The stencil thickness may need to be reduced when using finer pitch BGA parts. Stencil thickness and land size will determine paste volume, which is very critical for ceramic BGAs. It is helpful to have trapezoidal stencil apertures (slightly larger opening on the bottom than on the top) for better paste release.

Generally, on larger BGA components with 1.25 mm and 1.00 mm pitch, the aperture is large enough that stencil clogging, print registration and definition are less of a problem than with QFP components.

3.1.4 Inspection Requirements As with any surface mount part, BGAs should not be moved after component placement because this may smear the paste and cause solder bridges. The outline of the component can be included in the silk screen to show gross alignment problems, but the parts will self align during reflow if not more than 50% off the land. If a BGA has a gross misalignment problem it should be removed before reflow and reworked later. Though it may not be practical for high volume production, using X-ray or optical inspection (endoscope) to inspect failures before removing the part may be desirable.

3.1.5 Test Test strategies need to be developed before using BGAs. The solder joints cannot be probed and test

points are required. It may be difficult to incorporate enough test points to adequately test all solder joints. Some alternative test strategies may be needed. Some BGA components may have boundary scan designed into them for increased test capability. Some BGA components have test points designed right on the top of the package. This is not a good practice, since it puts pressure on the BGA components and the joints.

3.2 Time to Market Readiness In some cases each designer will have an option to use or not to use BGA. The alternative may be using a high pin count QFP. However, if a company is new to BGA, it may take some time for the user and the suppliers of printed boards and assembly services to address the technical and business issues in order to implement BGA into products. It is very likely that time to market will be adversely impacted if both products and the technology are developed simultaneously. It is a good idea first to develop and validate the technology before implementing on a real product. Otherwise, if any problem develops in the product or technology, the deadline for product shipment will be missed. To assure time-to-market readiness, BGA implementation methodology and process steps should be analyzed.

3.3 Methodology In general, product design is cost, size, and/or performance driven; however, other considerations may be important. The product must also meet the thermal and environmental reliability requirements. These requirements can be met by various packaging options such as through-hole technology (TH), surface mount technology (SMT), fine pitch technology (FPT), ball grid array (BGA), chip scale packaging (CSP), flip chip technology or a combination of all these.

The designer faces a broad task. He or she must consider form, fit, function, cost, reliability, and time to market before choosing a particular course. A primary issue is the reliability of the final product. The product must function as intended in the working environment over the predicted life span of the equipment.

3.4 Process Step Analysis There are several available paths to utilizing BGA effectively. The length of each path depends on what design and assembly facilities a company presently has, and how quickly they can be made ready for production. The following is an example of one approach.

1. Select a list of candidate products for BGA.
2. Develop an equipment list based on the projected volume needs. If sufficient in-house expertise does not exist, it may be desirable to use a reputable training center or consultant to save cost and time.
3. Organize a team representing design, production, test, quality, and purchasing. This team is responsible for component and equipment selections and review.
4. Develop a comprehensive BGA design guide that stresses manufacturability. Use existing standards where possible.
5. Design the candidate products starting with the conversions of existing products using fine pitch components.
6. Conduct rigorous assembly and test reviews. Carefully monitor component purchasing to assure that components have the specified package, shipping method, metallization, solderability, and orientation in the shipping containers.
7. Develop comprehensive workmanship standards and a process control system that is statistically sound.
8. Design the remaining candidate products.

3.5 BGA Limitations and Issues Since BGA technology has moved into the mainstream there are still some decisions that need to be considered. These are business and technical issues that must be resolved. The areas of special concern are:

- Visual Inspection
- Moisture Sensitivity
- Rework
- Cost
- Availability
- Voids in BGA
- Standards and their adoption
- Reliability Concerns

BGA issues are not insurmountable, however they require dedicated engineering resources to develop and implement the process.

3.5.1 Visual Inspection BGA is not a package suitable for companies that assure quality by inspection and repair. BGA solder joints cannot be inspected unless X-ray or optical inspection techniques are used. To reap the benefits that BGA offers, robust process control must be maintained. Due to limited time and training, many companies find implementing such tight process control to be a difficult endeavor.

There are some visual inspections that would show good flow on an uncollapsed ball with ceramic BGAs, and also be able to show collapsed balls on plastic BGAs. Visual inspections of BGAs can identify problems with solder joints. Visual inspection of the outer rows serves as an indicator of some of these problems. Examples are; BGA alignment with the lands on the outer rows, or how the BGA is setting on the board, level or skewed.

3.5.2 Moisture Sensitivity The plastic BGA packages are very moisture sensitive. This makes them susceptible to warpage, swelling, pop corning, or cracking if the packages

are not properly baked and kept dry prior to package assembly. Component storage and handling procedures are critical for any moisture sensitive component including leaded surface mounted devices but it is critical for BGAs/ FBGAs.

Component moisture sensitivity is tested using J-STD-020. The moisture sensitivity level must be determined for each BGA package type. It is critical to know at which of the three temperatures, 220°C, 235°C, or 250°C, the BGA package was classified. The classification of the package type may drop several levels if the higher temperature is used.

Most laminate based BGAs cannot be mounted or classified at temperatures above 220°C. The hermetic Ceramic BGA are not moisture sensitive and therefore can be mounted using either of the higher temperatures. The industry is discussing doing testing at a higher temperature such as 260°C, which will create major issues with not only BGAs but also all surface mounted devices.

3.5.3 Thermally Unbalanced BGA Design The plastic BGA package is also susceptible to warpage during which the package edges lift up which could result in no connections on the outer rows. Package warpage is of real concern in flux only applications during rework. Large die sizes can cause CTE mismatch between the PCB and the package laminate material, which can create package warpage (see Figure 3-1).

Thermally unbalanced package designs, particularly those with heat spreaders on the top, will warp according to the classic bi-metal effect.

3.5.4 Rework Although BGAs do not require nearly as much rework as fine-pitch devices, many assemblers are apprehensive about using a component package that is difficult to be reworked. While BGA rework is difficult, it is by no means impossible. Tools and techniques for rework are becoming available that range from manual to automated techniques to reball the BGA or redress the land pattern.

Several factors must be addressed during the rework operation. These are:

- Number of heat cycles.
- Ball collapsed during reballing.
- No damage to pads on BGA interposer.
- No damage to lands on the product board.

3.5.5 Cost The BGA still has a slight cost differential compared to fine pitch peripheral packages that it replaces. However, competitive pressures keep bringing costs lower to meet new targets. Further costs accrue with the increased board layer counts that BGAs require, however there are many advantages to the interconnecting concepts and the performance characteristics resulting from BGA implementation.

Following are some of the key reasons for higher BGA package cost:

- Higher cost substrate (fine line/space).
- High T_g BT (bismaleimide-triazine) resin.
- Thermal enhancements.
- Electrical enhancements.
- Very fine external pitches.
- High temperature reflow requirements.
- Thin profile heights.

All of these have been addressed in the last few years and great progress has been made.

In general, it has been difficult to create standard pin count BGA designs because every die has different requirements. Each package/die combination is unique therefore economies of scale that manufacturers can achieve with perimeter leaded packages does not necessarily match the area array capability of the BGA.

Table 3-1 shows the expectations of the semiconductor industry as to what they expect to pay on a cost per pin relationship for the different technologies over the next several years. The shaded sections indicate a challenge and degree of difficulty in achieving the predicted goals. Table 3-1 is taken from the ITRS 2002 Roadmap and the costs are very aggressive. The lower range of costs reflect peripheral leaded packages and the higher ranges reflect array style packages like BGAs/FBGAs.

The opinion of many resource experts is that the prices in the future years may not be able to be achieved with profitability because of the low costs forecasted.

3.5.6 Availability The 1.5 mm, 1.27 mm, and 1.0 mm are available in high volumes in many locations in the world. These pitches are now mainstream and are common in the industry. The 0.80 mm to 0.50 mm pitch packages are becoming available and used in many advanced portable electronic applications.

3.5.7 Voids in BGA Many companies use x-ray, in-circuit test and automatic optical inspection in combination to improve their process control for BGA solder joints. Some look for voids through x-ray to determine accept/reject criteria. Some level of voiding in any kind of solder joint is inevitable.

There is still some debate as to what is an excessive void. The proponents of voids argue that it is not the void that is bad, but its location. For example, if the void is between the ball and the board, you essentially have nonwetting,

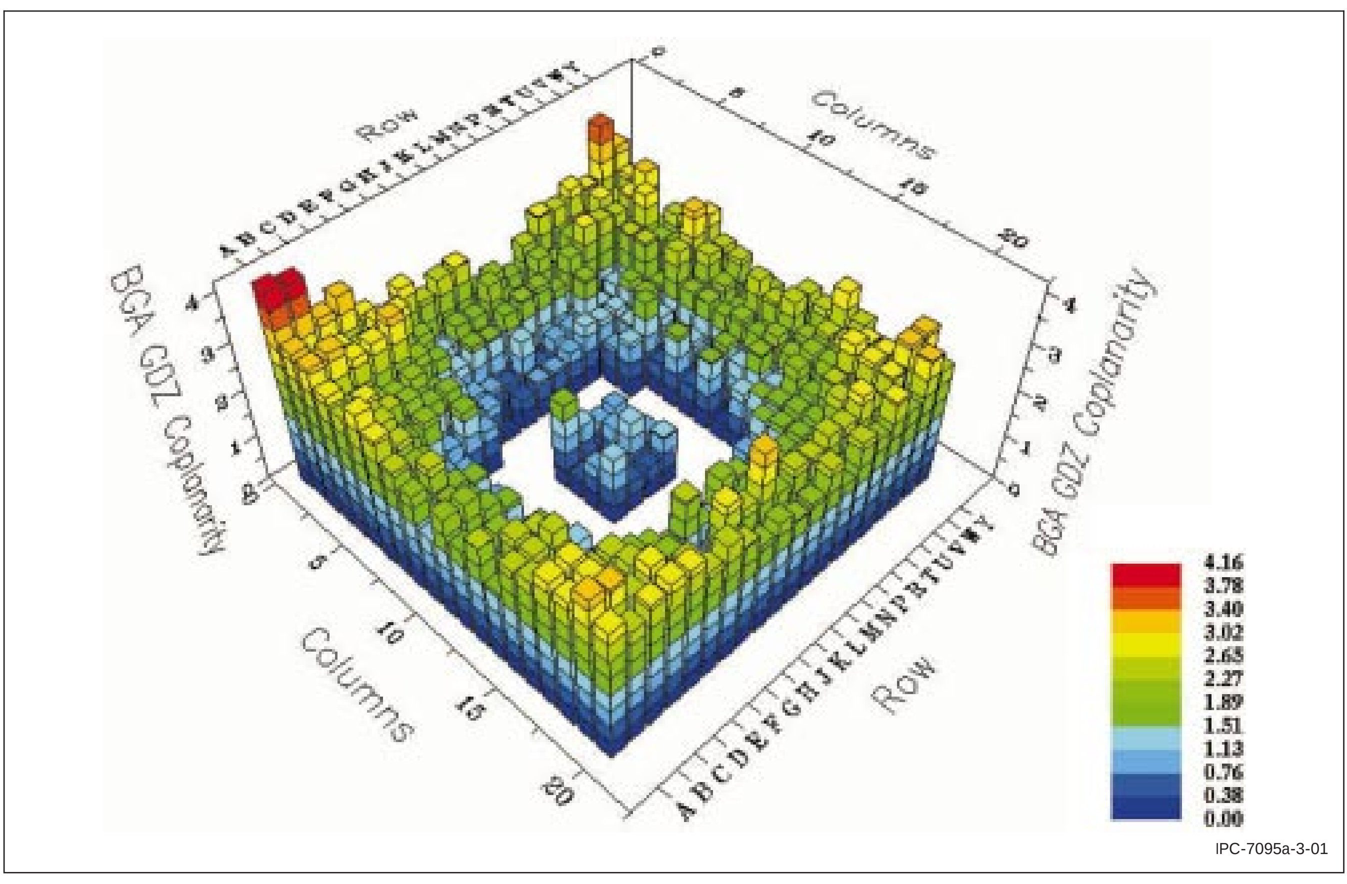


Figure 3-1 BGA Warpage

Table 3-1 Semiconductor Cost Predictions

Year Roadmap Input	2001 ITRS-99	2001 NEMI-00	2001 ITRS-01	2002 ITRS-01	2003 ITRS-01	2004 ITRS-01	2005 ITRS-01	2006 ITRS-01	2007 ITRS-01
Wafer Technology (nm)	180	180	130	115	100	90	80	70	65
Cost (Cents/Pin) (A)									
Low-Cost	**0.36-0.81**	**0.36-0.81**	**0.30-0.75**	**0.28-0.68**	**0.26-0.62**	**0.25-0.56**	**0.24-0.51**	**0.23-0.46**	**0.22-0.41**
Hand-Held	**0.45-1.17**	0.45-0.95	0.45-0.90	0.42-0.81	0.40-0.73	0.38-0.65	0.36-0.60	0.34-0.56	0.32-0.52
Cost-Performance	**0.81-1.71**	0.81-1.33	0.80-1.60	0.75-1.44	0.70-1.30	0.66-1.17	0.61-1.06	0.56-1.03	0.53-1.00
High-Performance	**2.80**	2.80	**2.20**	**2.09**	**1.98**	**1.88**	**1.78**	**1.69**	**1.61**
Harsh	**0.45-0.90**	0.45-0.90	0.45-4.00	0.40-3.60	0.36-3.20	0.32-2.88	**0.29-2.59**	**0.26-2.33**	**0.23-2.11**
Memory	**0.36-1.54**	**0.36-1.54**	0.36-1.54	0.34-1.39	0.32-1.26	0.30-1.14	**0.28-1.03**	**0.27-0.93**	**0.27-0.84**

White – Solutions exist **Yellow** – Solutions being pursued **Red** – No known solutions

which is unacceptable. Most voids in BGA are in the ball, well above the board, and hence the nonwetting or dewetting analogy is inappropriate.

3.5.8 Standardization Issues Many of the BGAs are using conventional printed board (interposer) materials, but are being tested to the standard component reliability tests. Standardization efforts are being undertaken by both JEDEC and IPC to test these new packages to the requirement limits of the bulk of the applications. The majority of these packages are going into office equipment, laptop computers and portable electronic applications that do not require the life cycle performance requirements needed by other applications.

Application specific qualification standards are needed to relate the test conditions to the environment in which the product will be used. Many of the industry technology roadmaps have identified these environments as being low cost benign, hand held, high function hand held, cost performance, high performance and harsh environments. Only the components used in harsh environments require some of the Highly Accelerated Stress Testing (HAST) presently being imposed on many of the constituents of the BGA.

3.5.9 Reliability Concerns Reliability issues relate to the component and the component mounted on an interconnecting substrate, usually an organic printed board. The component reliability issues are addressed through proper mounting of the die to the interposer that transfers the die bonding sites to the area array format used as the mounting structure within the component. Wire bonding techniques have been used for many years to attach die to lead frames.

The processes are well known, and when used in a BGA configuration afford high yields. Another popular technique is to mount the bare die face down onto the interposer in a flip chip configuration. Using flip chip processes requires a tighter control of the land positions on the interposer so that the lands line up properly with the bonding sites on the bare die. In addition, if the interposer is made of organic materials the attachment process also requires underfill in order to capture the joints so that the CTE difference does not impact the joint integrity.

Thick gold (more than 0.25 µm) as a surface finish should be avoided due to the risk of gold embrittlement since sufficient solder volume may not be available.

4 COMPONENT CONSIDERATIONS

4.1 Component Packaging Comparisons and Drivers

4.1.1 Package Feature Comparisons There are many types of package formats for ICs but only four types of terminal shapes; in-line pin (both single and dual), pin grid array, J lead, and gull wing lead. The most common lead configurations for surface mountable plastic packaged ICs are the J lead and gull wing lead. Of these two, the gull wing lead form is the most commonly used lead type for plastic packaged ICs. One of the biggest problems with gull wing leads is their fragility and, consequently, susceptibility to lead damage such as coplanarity, lead bending and sweep.

Lead damage is one of the leading causes of defects in gull wing leaded packages. Although gull wing devices are the most commonly used lead form for low and high pin count packages, ball grid array packaged devices have achieved broad acceptance due to its physical robustness, (pin-for-pin) size reduction and enhanced electrical performance.

In regard to performance, the BGA signal paths can be much shorter than those of fine-pitch gull wing lead package, advantageous in high-speed applications. BGA packaged ICs have exhibited very high board level assembly process yield due to their ability to self-center during reflow soldering. Because the array format can accommodate high I/O within a small form factor, BGA has proved to be a practical solution to the high pin count packaging trend as well.

Nonsymmetrical ball patterns have the added advantage of enabling automated orientation detection during assembly. One example is to omit one of the corner balls in an otherwise symetrical array.

4.1.2 BGA Package Drivers The emphasis on faster, smaller and lighter electronics systems is making component, board and system packaging more complex. The increase in assembly complexity is due in part to the wide use of small outline surface mountable packages, the key to miniaturization of electronics products. The device contact pitch plays a critical role in the complexity of manufacturing process as well. For example, with the adoption of finer and finer contact pitches, greater precision is demanded for each process in the assembly sequence; pick-and place, solder paste printing and, solder reflow. Inspection, rework and repair become more precise as well.

Key issues to be addressed when selecting BGA component packaging are thermal and electrical performance, real estate constraint and cost. The component packaging requirement varies for different types of systems. For example, the high-end microprocessors run at higher frequencies and require thermally and electrically enhanced packages. Examples of thermal enhancements are heat slugs, heat spreaders, heat sink and fin-fan (fan mounted on heat sink) etc. And examples of electrical enhancements are multilayer and higher pin-count packages and in-package capacitance. Hermetic ceramic packages are generally used for the in-package capacitance application. For mid-range systems, performance is important as well, but so is cost (not that cost is not important for high end systems).

4.1.3 Cost Issues Lead-frame packaged ICs have traditionally maintained a relatively low manufacturing cost. This is due to the very high volume of products being offered in a limited package configuration. This allows the manufacturer to utilize common tooling and molding processes for a diverse number of customer applications. The array package format, on the other hand, is more often designed and engineered for a specific product application. The initial cost for packaging BGA devices with a pin count of less than 200 will most likely be greater than lead-frame packaging. This is due in part to the unique single application substrate design and additional package assembly process steps. Cost parity between lead frame packaged ICs and the BGA package is generally reached when the device requires 200 or more I/O.

4.1.4 Component Handling BGAs can be furnished in a carrier tray format or tape-and-reel. The EIA standard embossed tape-and-reel format is often specified when the IC components are relatively small and/or required for very high-volume applications.

The JEDEC registered carrier trays are furnished to meet industry developed design guidelines (see JEDEC publication 95, Section 4.9 and Section 4.10) with a fixed length,

width, and thickness. The plastic packaged ICs, including the BGA, are susceptible to moisture retention that can damage the package during reflow solder processing. To protect the devices from undue physical contact and exposure to humidity, the loaded carrier trays are shipped in a sealed ESD and vacuum purged moisture resistant envelope (and should remain sealed until ready for board level assembly, see 4.8.5).

It is recommended that the user specify that plastic encased BGAs be furnished in the tray format rather than the tape-and-reel format. The tray carrier will accommodate the potential need to bake-out devices that are prone to moisture absorption. For example, if the plastic BGA packages are exposed to ambient conditions for more than twenty-four hours they will likely require baking before assembly. The plastic tray carriers developed for bake-out are rated to withstand 125°C temperature. The tape and reel materials, on the other-hand, cannot be exposed to temperatures above 50°C without damaging the carrier tape. So baking a moisture sensitive BGA in the tape format could take many days (see 11.1 for additional requirements).

4.1.5 Thermal Performance Thermal enhancements have become essential with introduction of faster and faster microprocessors. With introduction of new generations of microprocessors, power dissipation has continually moved upward. As the device clocking speed increases, the power goes up. The problem of higher power is mitigated, fortunately, with ''die shrink'' made possible by the reduction of transistor feature sizes in contemporary semiconductor processes and the associated trend towards lower power supply voltages. (As device geometry shrinks, the field intensities increase, promoting a reduction in supply voltages to avoid destructive effects.) The ceramic BGA is commonly used for higher wattage packages, as it has greater thermal conductivity than plastic packages. Plastic packages, however, are also evolving, and thermally enhanced plastic packages are already in wide use by the industry. Thermally enhanced plastic packages used to be limited to 6 - 8 watts, however, by incorporating integral metal heat spreaders, plastic packages can accommodate up to 30 watts.

4.1.6 Real Estate Real estate constraint is one of the important driving forces in reducing component package size. This has contributed to the widespread usage of surface mount devices, which are not only smaller in size, but enable component mounting on both sides of the board. As pin counts increase, however, even with surface mount, the conductor-to-conductor pitch must decrease to keep the size of the package within a practical range for manufacturing.

As the pitch of the BGA package decreases, the opportunity for placing more components in a given area increases. Although the board real estate can now support more functions per unit area, components such as the FBGA (fine pitch BGA) are more difficult to interconnect. This fact may increase the number of conductive layers required for the total circuit. Thus, surface real estate is optimized at the expense of more conductor routing layers.

4.1.7 Electrical Performance Electrical performance drivers include signal fidelity, operating frequency, power, and pin-count. With increasing frequency, the need for improved impedance control and minimal package insertion loss are a concern. With impedance control comes the need for terminations to prevent or dampen reflections. These terminations, if performed in parallel to source and/or load points on critical signals, will increase power consumption. High frequency operation itself, all other things being equal, drives power consumption upward with the square of frequency. As such, low power semiconductor research is increasing, in an attempt to reduce the average power consumption of complex digital ICs. Fortunately, as IC processes mature, the power per logic operation decreases by virtue of smaller device feature sizes. In the case of ceramic packages, even with increase in bond lands for high-speed devices, the pin count growth required for power and ground distribution is kept to a minimum by exploiting the intrinsically high package capacitance and employing package-mounted bypass capacitors.

4.2 Die Mounting in the BGA Package There are many ways a die is mounted in a BGA. The three main variations can be differentiated by the medium of signal transmission from the die to the solder ball array. In the basic three designs, the signal is carried by wire, conductive material (flip chip) or conductive ribbon-lead. The substrate can be ceramic or organic. The package properties will depend on the properties of the substrate material and its dimensional parameters. The following descriptions represent the more common methodology for die-to-package assembly.

4.2.1 Wire Bond There are two main forms of the wire bonded BGA. They are chip-on-board (COB) with the active surface of the die facing away from the substrate and board-on-chip (BOC) types with the active surface of the die facing the substrate. In this structure the bond pads on the die are generally furnished at its periphery and the wire bonds are made from the die periphery to the pads on substrate surrounding the die.

The die can be attached to the substrate using conductive or nonconductive adhesive. Use of electrically conductive adhesive is specified when the die backside requires an electrical connection. The drawback is that the substrate area under and equivalent to the size of the die cannot be accessed for in-package circuit routing. If the die does not

require a backside electrical connection then a nonconductive adhesive can be used to place the die on the substrate. In this case, the area under the die can be used for signal routing.

The adhesive selected for die attach must not adversely affect the mechanical integrity of the traces or the integrity of the electrical signal. Following die attach and adhesive curing process the die is ready for electrical interface to the substrate base. The bond pads on the die are connected electrically to the bond pads on the substrate using gold wire or aluminum wire where feasible. The traces on the substrate route the signals from wire bond pads to ball grid array on the bottom of the substrate through plated via holes. Following the wire-bond process, the die and bond area is typically protected by encapsulation, conformal coating or plastic over-mold. The encapsulation can be applied in the form of glob top or it can be molded in a press. An alternative to encapsulation is the post-assembly attachment of a premolded cover.

In the BOC or die face-down structure, the bond pads on the die can be located at the die periphery or in a row or rows at the center of the die. The substrate is designed with a narrow slot to accommodate the row or rows of bond pads on the die. The die-to-substrate adhesive is placed to the right and left of the bond pads. The adhesive can be applied in the form of a paste or a film. The active or circuit side of the die is attached face-down onto the substrate with the substrate slot exposing the bond pads on the die typical of that shown in Figure 4-1.

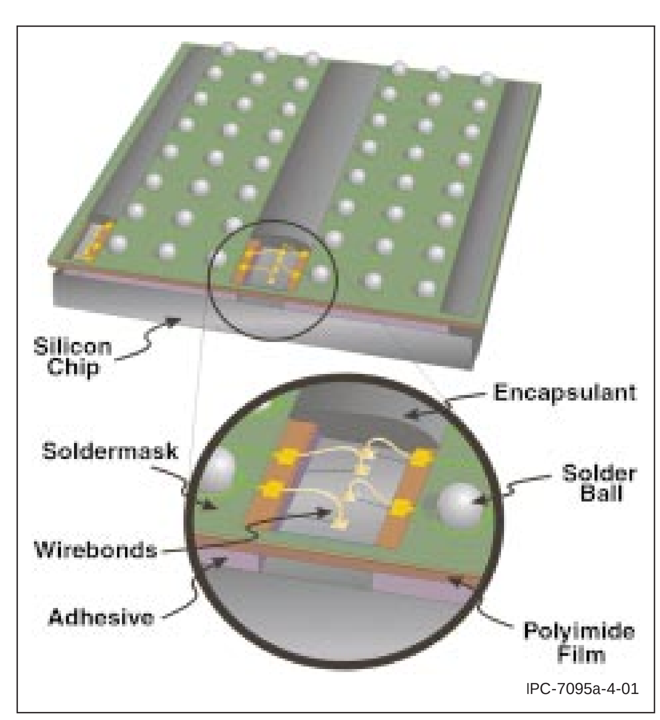


Figure 4-1 BOC BGA Construction

Following die attachment and adhesive cure, the bond pads on the die are wire-bonded to the corresponding pads surrounding the slot on the substrate. Following wire-bond, the wires and exposed die surface are encapsulated for protection. Note that one or more grid array rows will need to be depopulated to allow the slot in the substrate for wire-bond to the die. Also note that the wire bonding is accomplished at the center of the die and does not require additional peripheral area around it for die-to-substrate interface. Figure 4-2 illustrates the top and bottom of a mold-encapsulated BGA package.

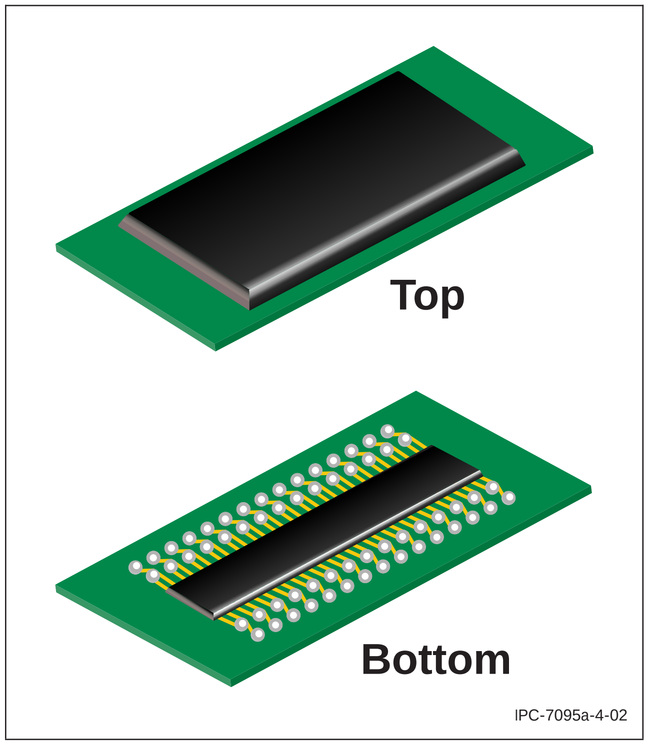


Figure 4-2 Top of Molded BOC Type BGA

4.2.2 Flip Chip The flip chip (or direct-chip-attach) design eliminates the need for wires and die attach. In this design, the prebumped die is flipped circuit side down and the lands on the circuit side of the die are brought into contact with corresponding lands on a substrate using solder or conductive adhesive. The die bond pads, however, are not immediately compatible with either solder or conductive adhesive attachment processes. Solder bumping with a solder compatible alloy composition before the die wafer is sawed is one of the most common procedures. The solder material and the bumped-pad structure materials are chosen to optimize electrical and mechanical connection.

Conductive adhesive or polymer attachment can be adapted as well, however, the die bump contact may require a ‘‘noble’’ alloy that is compatible with the conductive alloy particles in the adhesive. This alloy bump or ball can be applied to the die bond pads by plating or ball bonding processes. If a solder or an isotropically conductive adhesive is used, the gap between the die and the substrate may require an under-die-filling with epoxy to ensure mechanical integrity of the die-to-substrate interface. Use of an

anisotropically conductive material eliminates the need for added underfill. After attaching the die to the substrate, it is typically encapsulated, coated or over-molded for protection.

4.3 Standardization Standardization of BGA packaging has considered a number of physical variables including the diameter of the individual ball, the positional accuracy of the ball in relationship to a true position within the component outline.

4.3.1 Industry Standards for BGA For more detail regarding package variation, mechanical feature dimensions and allowable physical tolerances refer to the following JEDEC developed guidelines for BGA packaging.

4.3.1.1 BGA Package JEDEC Publication JEP95, Section 4.14, defines a Ball and Column Grid Array Package family. A Ball Grid Package (BGA) or Column Grid Array (CGA) is a square or rectangular 1.50, 1.27, & 1.00 mm pitch package with an array of metallic balls or columns on the underside of the package. The main body of the package has a metallized circuit pattern applied to a dielectric structure. To this package body, the semiconductor die(s) is attached to either the top or bottom surface. On the underside of the dielectric is an array pattern of metallized balls/columns which form the mechanical and electrical connection from the package body to a mating feature such as a printed circuit board. The surface that contains the die may be encapsulated by various techniques to protect the semiconductor.

4.3.1.2 Fine Pitch BGA Package JEDEC Publication JEP95, Section 4.5, defines a Fine-pitch Ball Grid Array (FBGA) package as a reduced-pitch (<1.00 mm) version of a Ball-Grid-Array (BGA) package. The carrier body of the package has a metallized circuit pattern applied to a dielectric structure. One or more semiconductor devices are attached to either the top or the bottom surface of this dielectric carrier. On the underside of the dielectric carrier is an array pattern of metallized balls, which form the mechanical and electrical connection from the package body to a mating feature such as a printed circuit board. The surface that contains the die may be encapsulated by various techniques to protect the semiconductor. The requirements for a square FBGA package family that allows four optional contact pitch variations; 0.50, 0.65, 0.75 and 0.80 mm and defines four device profile (height) variations as well. The 0.75 mm pitch has been added to the list thus providing four pitch variations for FBGA type parts.

The total profile height of the FBGA as measured from the seating plane to the top of the component, is >1.70 mm. The Low-Profile Fine-Pitch Ball-Grid-Array (LFBGA) is a *reduced-height* version of an FBGA. The total profile height of the LFBGA as measured from the seating plane to the top of the component, is no greater than 1.20 mm. Thin-Profile Fine-Pitch Ball-Grid-Array (TFBGA) is a *reduced-height* version of an FBGA with a total profile height as measured from the seating plane to the top of the component that does not exceed 1.00 mm and the Very-Thin-Profile Fine-Pitch Ball-Grid-Array (VFBGA) is a *reduced-height* version of an FBGA with a total profile height as measured from the seating plane to the top of the component that is at or below 0.80 mm.

The JEDEC design guide for FBGA allows the manufacturer the option to increase ball diameter as the spacing or pitch between ball contact centers increase as compared in Table 4-1. As of this release JEDEC standards do not support the 0.75 mm pitch, however the industry has some parts available in that pitch.

Table 4-1 JEDEC Standard JEP95, Section 4.5 Allowable Ball Diameter Variations for FBGA

Ball Pitch	Ball Diameter/mm		
	Min	Nom.	Max.
0.50	0.25	0.30	0.35
0.65	0.25	0.30	0.35
0.65	0.35	0.40	0.45
0.80	0.25	0.30	0.35
0.80	0.35	0.40	0.45
0.80	0.45	0.50	0.55

The larger ball diameter option has been allowed to accommodate packages using rigid interposer structures. The larger diameter ball may compensate to a degree, for the wide mismatch of the coefficient of thermal expansion (CTE) between the silicon die and the rigid PCB structure.

4.3.1.3 Fine Pitch Rectangular BGA Package JEDEC Publication JEP95, Section 4.6, defines a Fine-pitch, Rectangular Ball Grid Array (FRBGA) has an array of metallic balls on the underside of the package. The substrate or carrier of the package has a rectangular shape with a metallized circuit pattern applied to either or both sides of a dielectric structure. Generally described with the same general terms noted in the JEP95, Section 4.5, the body size for an FRBGA is defined by the D and E dimensions. Dimension D is the size of the body when measured parallel to the major axis of the package and dimension E is the size measured parallel to the minor axis. Thus, for rectangular packages D will have a larger value than E.

4.3.1.4 Die Size BGA Package JEDEC Publication JEP95, Section 4.7, defines a Die-size Ball Grid Array (DSBGA) package. A Die-size Ball Grid Array has an array of metallic balls on the underside of the package. The substrate or carrier of the package may have a square or rectangular shape with a metallized circuit pattern applied to

either or both sides of a dielectric structure. The semiconductor die is attached to the top surface of this dielectric carrier. On the underside of the dielectric the array pattern of metallized balls provides the mechanical and electrical connection from the package body to the next level component such as a printed circuit board. The surface to which the die is attached may be encapsulated by various techniques to protect the semiconductor. The size of the substrate or carrier is as close to the die size as practically possible.

A ''die-size'' ball grid array (DSBGA) is a type of BGA package where the body size is defined to coincide as closely as possible with a specific die size. This package is sometimes called a ''real chip-size'' BGA or CSP. The dimensions of the package body accommodate assembly only of a die with a specific size, and these body dimensions will change as a result of future changes in die size. The outline of the package may be square or rectangular, but this aspect ratio may also change as a given package is redesigned to conform to a new die size. The aspect ratio will likely differ for devices of the same functionality from multiple suppliers. The controlling factor for the standardization of DSBGA packages is the size and aspect ratio of the ball array.

The D and E dimensions define the body size for a DSBGA package. For packages with a rectangular ball matrix, the matrix determines the orientation of the dimensions. Dimension D is the body size measured parallel to the major axis of the ball matrix, and dimension E is the body size measured parallel to the minor axis of the ball matrix. Thus, for rectangular packages D will not necessarily have a larger value than E as would be the case for an FRBGA package per JEDEC JEP95, Section 4.6. A DSBGA package with a square ball matrix should follow the usual JEDEC convention where D is greater than E. The maximum values for both D and E are defined in JEDEC Publication 95 using 0.50 mm increments. The values are determined by rounding the actual DSBGA body size upward to the next 0.50 mm boundary. Thus, D and E values have the form y.00 or y.50 following this procedure.

The array pitch for a DSBGA package will not necessarily be equal for the D and E matrix dimensions. When the pitches are not equal, ball dimensions and tolerances for the smaller of the two pitches will govern the definition of related package dimensions and tolerances. The controlling pitch of the array of balls on a DSBGA package is always less than 1.0 mm. The contact pitch variations for the DSBGA described in JEP95, Section 4.7, are 0.80, 0.75, 0.65 and 0.50 mm.

4.3.2 Ball Pitch Ball Grid Arrays are divided up into two groups of pitches. The first group includes both plastic and ceramic package outlines allowing 1.50, 1.27, and 1.00 mm contact pitch variations. The second group is designated as a fine-pitch BGA package family allowing ball contact pitch variations of 0.80 mm, 0.65 mm, 0.50 mm and 0.40 mm. Few component manufacturers are currently providing parts with 1.5 mm pitch, as the pressure is on form factor in order to keep BGAs as small as possible and although ball pitch of 0.40 mm and less are allowed, the applications may be limited for conventional surface mount assembly due to difficulty in processing. Pitch plays a large role in the determination of what ball diameters can be used in various combinations. Table 4-2 shows the characteristics of those balls that are used with pitches of 0.5 mm through 1.5 mm.

Table 4-2 Ball Diameter Sizes for PBGAs

Nominal Ball Diameter (mm)	Tolerance Variation (mm)	Pitch (mm)
0.75	0.90 - 0.65	1.5, 1.27
0.60	0.70 - 0.50	1.0
0.50	0.55 - 0.45	1.0, 0.8
0.45	0.50 - 0.40	1.0, 0.8, 0.75
0.40	0.45 - 0.35	0.80, 0.75, 0.65
0.30	0.35 - 0.25	0.8, 0.75, 0.65, 0.50

4.3.2.1 Future Ball Contact Size Conditions Although not required for the BGAs shown in Table 4-2, future ball sizes contemplated are shown in Table 4.3.

Table 4-3 Future Ball Size Diameters for PBGAs

Nominal Ball Diameter (mm)	Tolerance Variation (mm)	Pitch (mm)
0.25	0.28 - 0.22	0.40
0.20	0.22 - 0.18	0.30
0.15	0.17 - 0.13	0.25

4.3.2.2 Land Pattern Approximation The land pattern of the component substrate (where the ball is attached) and the land pattern of the mounting structure (printed board) should be as similar in diameter as possible. Component manufacturers have determined that the land pattern or pad on the component should be slightly less than the ball diameter. The amount of reduction is based on the original ball size, which is used to determine the average land. In determining the relationship between nominal characteristics, a manufacturing allowance for land size has been determined to be 0.1 mm between the Maximum Material Condition (MMC) and Least Material Condition (LMC).

The information shown in Table 4-4 provides data on land patterns and their variation to accommodate six common ball diameters.

Many component manufacturers use solder mask-defined lands (see 6.2.2). When this technique is employed, the nominal land diameter should be increased by the amount of solder mask encroachment on the land (usually about 0.1

Table 4-4 Land Size Approximation

Nominal Ball Diameter (mm)	Reduction	Nominal Land Diameter (mm)	Land Variation (mm)
0.75	25%	0.55	0.60 - 0.50
0.60	25%	0.45	0.50 - 0.40
0.50	20%	0.40	0.45 - 0.35
0.45	20%	0.35	0.40 - 0.30
0.40	20%	0.30	0.35 - 0.25
0.30	20%	0.25	0.25 - 0.20

mm). The opening in the solder mask window, then represents the diameter to which the ball will become attached, while the actual land is slightly larger to accommodate the solder mask-defined land concepts. It should be noted that routing density is decreased, since the land is larger. Table 4-5 shows future land size approximations. These indications are for ball sizes from 0.25 mm to 0.15 mm. The same relationships for a solder mask-defined land applies as stated for Table 4-4.

Table 4-5 Future Land Size Approximation

Nominal Ball Sizes (mm)	Reduction	Nominal Land Size (mm)	Land Variation (mm)
0.25	20%	0.20	0.20 - 0.17
0.20	20%	0.15	0.15 - 0.12
0.15	20%	0.10	0.10 - 0.08

4.3.3 BGA Package Outline Body sizes for Ball Grid Arrays are divided up into the following two outline groups: Square and Rectangular. The Square outline package family size ranges from as small as 4 mm x 4 mm and as large as 50 mm x 50 mm. In the fine pitch variations you will see the package sizes increase in 1.0 mm increments. In the ranges above 21 mm x 21 mm you will see the body size increase in increments of 2.0 mm to 2.5 mm and the pitches are in the regular range. Rarely will any of the fine pitch parts be found in sizes larger than 21 mm x 21 mm. The Rectangular BGA family has the same size ranges from 4.0 mm to 50 mm but varies by each application. This group can have many more variations than the square group. Rectangular sizes typically are found to follow no fixed incremental progression. This group is normally driven by the Memory applications and closely follows the die sizes. Rectangular sizes are normally standardized in small application specific families. The fine pitch BGA components, equal to or less than 0.8 mm, rarely exceed 21 mm in body size.

Fine Pitch Ball Grid Arrays (FBGA) is a 0.40 to 0.80 mm pitch solder balled array package that has fixed package dimensions ''D (Length)'' and ''E (Width).'' The FBGA is more like the plastic and ceramic BGA families described above having fixed body dimensions. Although the FBGA outline is typically only 20% larger than the die, it will not change shape with every die shrink.

The Die Size Ball Grid Array Package (DSBGA) is a 0.50 to 0.80 mm pitch solder balled array package that has variable package dimensions ''D (Length)'' and ''E (Width).'' The DSBGA package takes the shape of the die which normally makes it a rectangular outline and is presently widely used in Flash and DRAM Memory devices. The Rectangular Die Size (RDS) outline will likely change ''D'' and ''E'' dimensions with every die shrink.

4.3.4 Ball Size Relationships The total variation of the system considers three major issues: positioning, ball tolerance, and substrate tolerance. All three attributes added together result in a worst case analysis, however as with other land patterns in the standard, a statistical average is determined by using the RMS (root, mean, square) value. Table 4-6 shows the total variation in the system for each of the nine ball sizes identified in the standards. As noted, the standard nominal dimension for ball contact diameters are 0.15, 0.20, 0.25, 0.30, 0.40, 0.45, 0.50, 0.60, and 0.75 mm. Ball contact size for array packages are influenced by the limit established for overall package height, ball contact pitch and the desire to maximize solder joint reliability.

4.3.5 Coplanarity A critical issue in surface mount packages is the limits for coplanarity of the contacts. The coplanarity requirements in BGA are very different from other lead-frame packaged surface mount components. Coplanarity for BGA is the distance of component contact surface above a common seating plane. Thus, noncoplanarity, a simplified term, is the maximum distance between the lowest and the highest pin when the package rests on a perfectly flat surface. This definition represents a package sitting on a PC board on at least three leads.

Coplanarity tolerance defines the distance from the seating plane to the highest point of the package. This dimension includes the standoff height, package body thickness and (if present) lid thickness. The measurement criteria do not include attached features such as heat sinks or other components. An integral heatslug, however, is not considered an attached feature. If the package happens to be laminate substrate based BGA, additional coplanarity issues can be expected due to problems associated with adapting larger substrates and maintaining flatness within tolerances. This, in part, is reason why the plastic BGA package coplanarity requirement is established at 150 µm. Most suppliers would like the allowable BGA coplanarity limit to be around 200 µm but the users would prefer the maximum to be no greater than 100 µm (see 4.6.2.6 and 4.8.4).

There are different coplanarity requirements for different types of BGAs. The following examples are a sampling of JEDEC registered BGA package outlines:

Table 4-6 Land-to-Ball Calculations for Current and Future BGA Packages (mm)

RLP	Land Size		Location Allowance	Ball Variation	PCB Fabrication Allowance	Ball Size			% Reduction From Nom.	Variation Allowance
	MMC	LMC				Nominal	MMC	LMC		
050	0.60	0.50	0.10	0.25	0.10	0.75	0.90	0.65	25%	0.25
051	0.50	0.40	0.10	0.20	0.10	0.60	0.70	0.50	25%	0.20
052	0.45	0.35	0.10	0.10	0.10	0.50	0.55	0.45	20%	0.17
053	0.40	0.30	0.10	0.10	0.10	0.45	0.50	0.40	20%	0.17
054	0.35	0.25	0.10	0.10	0.10	0.40	0.45	0.35	20%	0.17
055	0.25	0.20	0.05	0.10	0.05	0.30	0.35	0.25	20%	0.15
056	0.20	0.17	0.05	0.06	0.03	0.25	0.28	0.22	20%	0.08
057	0.15	0.12	0.05	0.04	0.03	0.20	0.22	0.18	20%	0.07
058	0.10	0.08	0.05	0.04	0.02	0.15	0.17	0.13	20%	0.07

Registered Outline	Package Type	Coplanarity
MO-151	Plastic BGA	0.20 mm
MO-156/ MO-157	Ceramic BGA	0.15 mm
MO-195	Fine Pitch BGA	0.08 mm

The coplanarity values may vary from JEDEC Outline to Outline because of the ball metallurgy. In low temperature, eutectic (183°C melting point) solder balls, the balls collapse during the assembly operation, therefore the coplanarity requirement is not as tight as a high temperature (302°C melting point) solder balls in which the balls do not collapse during the assembly operation.

4.4 Component Packaging Style Considerations The JEDEC Design Guidelines for BGA do not define specific materials or method of assembly. The base material will vary from one supplier to another depending on application. The base structure is most likely a reinforced organic laminate, a nonreinforced polyimide film or ceramic. Ceramic based BGA package is often supplied with noncollapsing solder balls made of high temperature solder (90% lead, 10% tin) with melting point of 302°C. The ball size will vary with the pitch and package size. Larger packages will usually have larger ball sizes to improve reliability. Since the ceramic package is relatively very flat, and the tolerances in ball diameters are very narrow, the coplanarity requirements can be relatively narrow as well. The supplier of the ceramic-based package will generally furnish recommendations for selecting a suitable solder paste composition for board level assembly.

Laminate and Polyimide Film based BGA is very different, however. The laminate based package is essentially made of circuit board material with a high temperature (T_g) rating. A high T_g rated resin system adopted by several companies for BGA package applications is bismaleimide triazine (BT). Reinforced polyimides and polyimide films have an even higher temperature rating and are also in wide use for both BGA and FBGA.

4.4.1 Solder Ball Contact Alloy The alloy composition selected for ball contacts on reinforced laminate and polyimide film based BGA packages can vary a great deal. Many are furnished with a eutectic solder having a melting (liquidus) point of 183°C (or 179°C for eutectic solder with 2% silver). The ball contacts are commonly applied to the package substrate using only flux and a reflow soldering temperature of 215-220°C to complete the joining process.

4.4.1.1 Lead Free BGA Contacts For applications requiring a lead free alloy composition, tin, silver or tin, silver, copper alloys are combined for both solder ball contacts and solder paste. These solders have liquidus temperatures in the range of 210 to 227°C and require peak reflow temperatures in excess of 240°C; corresponding maximum package temperatures may be as high as 260°C. BGA packages may be supplied with ball contacts that use an alloy composition that is not designed to reach a liquidus stage. In this application, the noncollapsing ball contact is attached to the package with solder paste composition typical of that used for board level assembly.

4.4.2 Ball Attach Process The package substrate is typically fabricated in a strip format containing multiple packages. Ball contact placement is performed after they have gone through wire bonding and plastic molding or encapsulation process steps. Both automated and semiautomated ball placement is being utilized for volume BGA assembly. Alloy spheres of the desired size (as shown in Table 4-1) are attached either by gang placement machines or dispensed in mass with a stencil-like fixture. For companies doing development or for low-volume placement, simple template fixtures can be provided for precise ball positioning. The overall ball attachment process, however, is the same. To begin, liquid or paste flux is dispensed or printed onto the contact pattern. The flux holds the balls in place during reflow soldering. Reflow soldering of the ball to the substrate is often performed in a nitrogen gas environment. The nitrogen gas environment helps provide consistent ball quality and keeps the surface from oxidizing during reflow. However, nitrogen gas may not be necessary for reflow attachment of the package to the PCB. The eutectic solder

balls provide a ‘‘controlled collapse’’ that, during reflow soldering, promotes self-alignment (compensating for some misplacement during assembly).

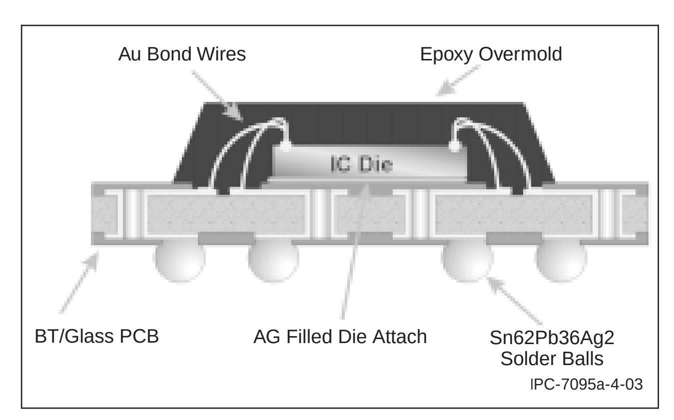


Figure 4-3 Cross-Section of a Plastic Ball Grid Array (PBGA) Package

There are some issues to consider when adapting plastic BGA packaging, moisture sensitivity and rework following removal. The plastic cased BGA will require specialized tooling and skills to reball after the package is detached from the board assembly. This may not be the case with the high melting point noncollapsing balls used on ceramic based BGA because they do not melt during rework.

The plastic BGA package is also susceptible to warpage when exposed to temperatures required for solder attachment. The edges of the package tend to lift up or curve down during reflow soldering and can severely disturb or interrupt the electrical interface between package and board assembly. The larger packages are even more susceptible to warpage than the smaller packages. The package warpage is caused by CTE mismatch between the substrate structure, the mold compound and the silicon die inside. This problem may become more acute when the die is large, or when the BGA has a heatspreader.

4.4.3 Ceramic Ball Grid Array The internal connection in the ceramic-based package can be either wire-bond or flip-chip. Figure 4-4 shows flip-chip bonding inside the package. The package can be furnished with the die mounted on the top surface of the substrate (cavity up) or with the die mounted to the substrates lower surface (cavity down). The solder balls generally used for ceramic package applications are a high temperature alloy composition (90% lead and 10% tin) with a melting point of 302°C. The ball attachment alloy, however, may be a eutectic solder (Sn63Pb37).

Although plastic encapsulation or over-molding is widely used to encase the die area, some ceramic based BGA packaged devices are hermetic (do not absorb moisture). Also, since the solder balls have a high melting point, they do not collapse during rework and may not require reballing for reuse. The disadvantage of the ceramic-based

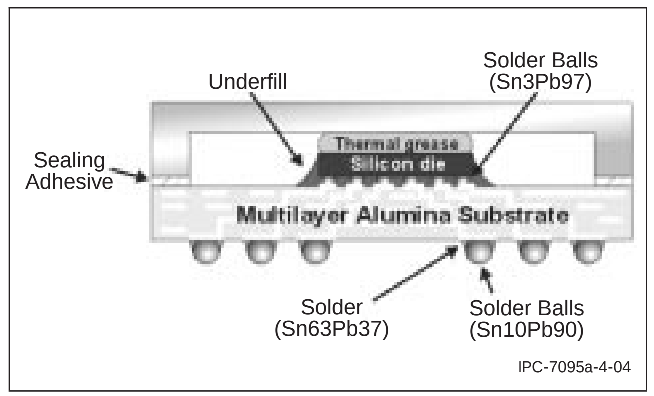


Figure 4-4 Cross-Section of a Ceramic Ball Grid Array (CBGA) Package

BGA is that its high thermal mass will be much different than the plastic packaged ICs and can make solder reflow profile development more difficult. The CTE mismatch between the ceramic-based package and the circuit board may need to be compensated as well. The solder attachment may not meet reliability expectations in more extreme environments without the use of an epoxy type underfill to stabilize and restrict movement in the component mounting area.

4.4.4 Ceramic Column Grid Arrays Solder column contacts typical of that illustrated in Figure 4-5 are used for larger ceramic-based packages (32 mm to 45 mm). The package resembles the earlier pin-grid-array but with closer contact pitch and more fragile leads (columns). The column contact diameter is approximately 0.5 mm with its length varying from 1.25 mm to 2.0 mm. The columns are attached to the package either by eutectic (Sn63Pb37) solder or they are cast in place using 90% Pb and 10% Sn. The longer columns typically increase solder joint reliability by absorbing a great deal of the stresses created by the CTE mismatch between the ceramic package and the board.

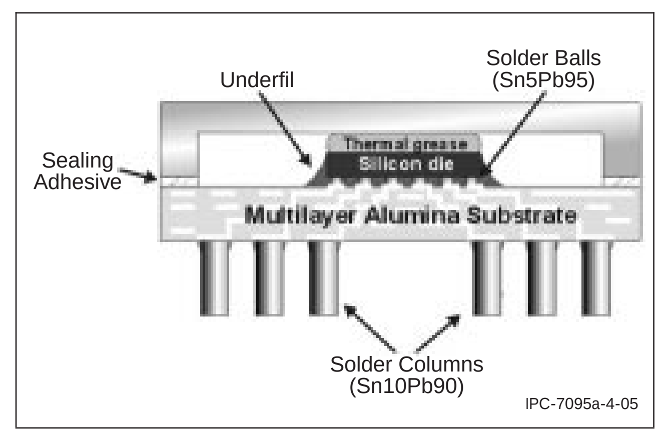


Figure 4-5 Cross-Section of a Ceramic Column Grid Array (CCGA) Package

Longer columns, on the other-hand, may reduce electrical performance and will increase the overall package profile.

Also the columns are not as rugged as ball contact and are susceptible to handling damage.

4.4.5 Tape Ball Grid Arrays Tape (polyimide film) based ball grid array shown in Figure 4-6, can furnish a lower overall profile package. The low dielectric polyimide film can be furnished with one or two metal layers for high density in-package circuit routing.

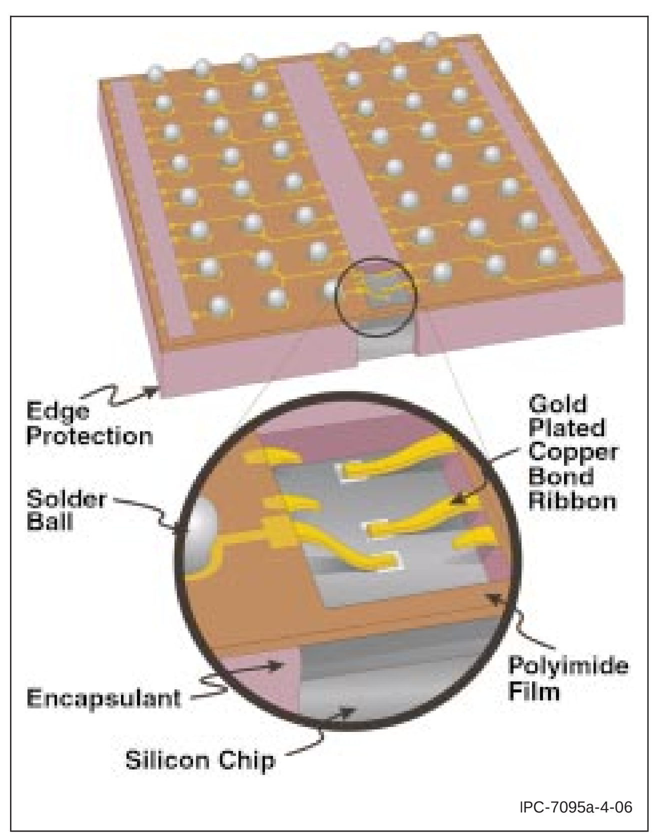


Figure 4-6 Polyimide Film Based Lead-Bond µBGA Package Substrate Furnishes Close Coupling Between Die Pad and Ball Contact

For polyimide-based BGA typical of that illustrated, the CTE mismatch is not an issue since the die attach adhesive and substrate flexibility will take up strains within the package structure. Tape-based BGAs can adapt flip-chip, wire-bond or lead-bond to achieve die-to-substrate interconnection. The single metal layer tape substrate is typically used for low cost and low lead count package applications and the two metal layer tape for higher lead count or performance driven applications.

An additional layer of copper, for example, can provide an efficient ground return, significantly lowering inductance and reducing the effects of switching noise. The ground plane effect impacts noise level reduction as well but the number of current sinks within the ground plane will also influence inductance levels. The two metal layer substrate compared in Figure 4-7 not only furnishes better electrical performance, it also provides a significant improvement in in-package circuit routability.

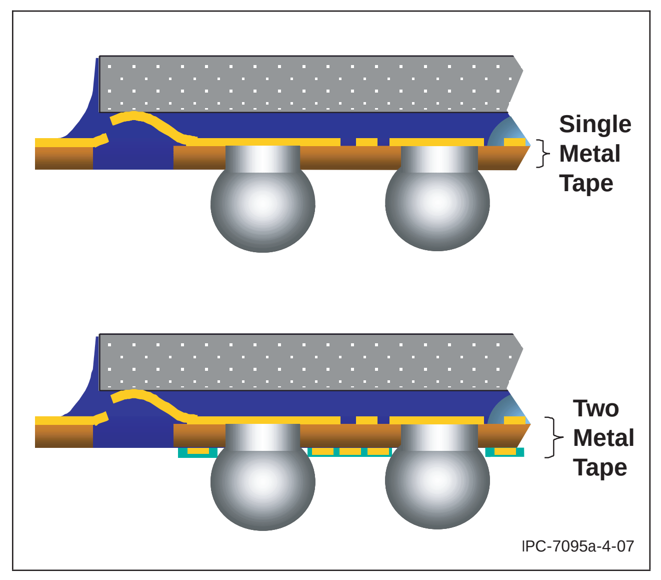


Figure 4-7 Comparing In-Package Circuit Routing Capability of the Single Metal Layer Tape Substrate to Two Metal Layer Tape Substrate

Circuit routing of the single metal material is limited to the narrow gap of dielectric between ball contact attachment sites. As the contact pitch reduces down to 0.50 mm, the space between contact features is reduced to 75 µm, providing the possibility of routing only a single circuit trace. This factor limits the use of single metal layer to a narrow band of low I/O package applications.

4.4.6 Multiple Die Packaging Portable and wireless electronics represent the most aggressive growth area for high-density package technology. In both circuit board fabrication and IC packaging, the technology for compressing even the most sophisticated electronic functions into a smaller and lighter finished product continues to evolve.

Portable or hand-held electronics are a natural target. Digital cameras and camcorders, for example, must consider ease of use, lighter weight and performance. Cellular phones, pagers, personal communicators, palm top computers, industrial and automotive electronics, personal GPS, medical and diagnostic products, are all viable candidates for more efficient device miniaturization.

Memory devices such as Flash, SRAM and SDRAM are the first commodity type products in the market to adapt FBGA and CSP in high volume. However, digital signal processors, controllers, CPUs and any number of application specific IC devices are also prime candidates for multiple die packaging. Many of the multiple die packages adapt a simple wire-bond process for die-to-substrate interface. The die and wire bond area is then encapsulated or over-molded to furnish the single package outline. Wire-bond solutions are capable of furnishing a two or three die stack but package height increases significantly with each added die layer.

Two and three ICs encased in a single package outline is more efficient in both size-to-function ratio and performance. Multiple die packaging potentially increases component density and improves component-to-component circuit routing efficiency on the printed wiring board. Some of the multiple die package methodologies attach one die on top of the other on a single substrate as illustrated in Figure 4-8.

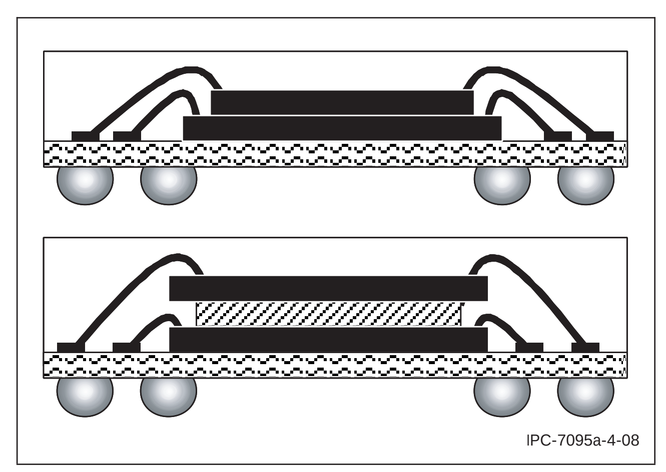


Figure 4-8 Single Package Die-Stack BGA

Die stacking different size die in a pyramid fashion is common but when the die are the same size, a spacer must be added between each active die to clear the wire-bond loop.

4.4.7 3D Folded Package Technology Memory die, such as Flash and SRAM, have relatively high fabrication yields. Damage can take place during assembly processing and handling but overall, the memory packaging process and testing has a very high pass ratio. Flexible substrate material enables the folding of several die into a single FBGA package outline that is only slightly greater than the largest die of the set.

Figure 4-9 is a typical folded-flex package application, combining three single memory function die into a single package outline.

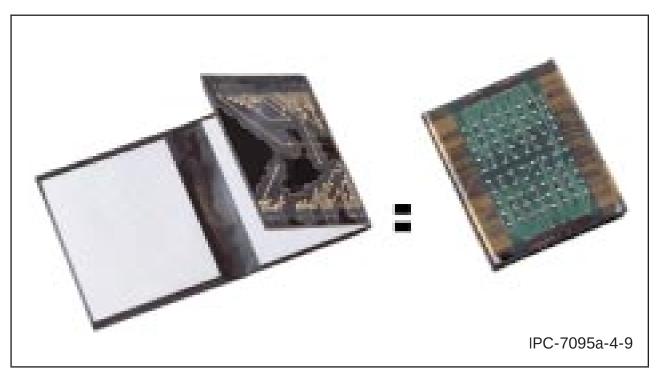


Figure 4-9 Folded Multiple-Die BGA Package

4.4.8 Ball Stack Packaging Although not limited to memory packaging, a key application is the stacking of DDR-SDRAM chips, which enables OEMs and memory module manufacturers to increase the density of their memory boards by up to eight times the current density available today. The stacking of pretested FBGA packaged die is an ideal application for memory. Testing, sorting and grading of memory before joining will ensure that the final component configuration furnishes its full performance potential. Figure 4-10 compares two and four section ball stack package variations for the center bond pad type memory.

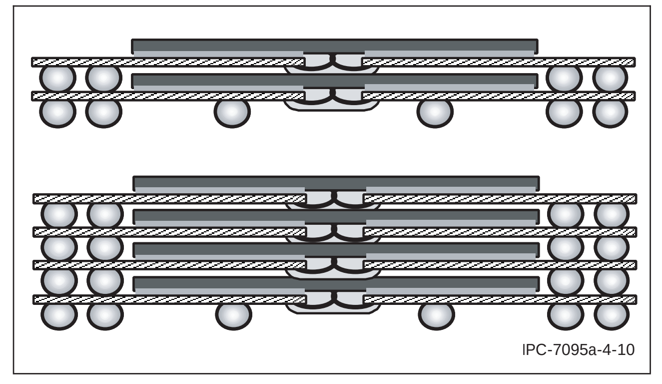


Figure 4-10 Ball Stack Package

Sequentially stacking one pretested FBGA package allows the dramatic increase in component density and functionality. As a practical example of a current application, consider the dynamics and potential for memory capacity on the standard single sided SO-DIMM shown in Figure 4-11.

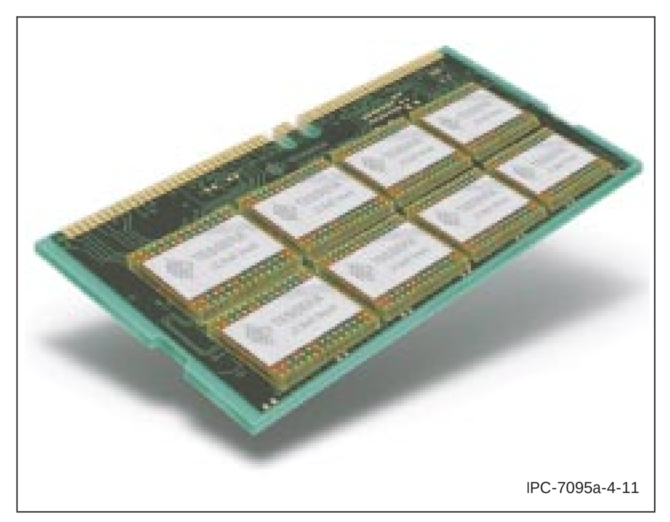


Figure 4-11 The Standard SO-DIMM Memory Card Assembly

4.4.9 Folded and Stacked Packaging Because processor and ASIC wafer fabrication yield is not as predictable as memory or less complex functions, pretesting of the individual die before package assembly is a must. In addition, combining two very different yielding products into the same finished package can be very risky. To minimize risk, the idea of building up the multiple-die package sequentially becomes highly attractive.

With the ultimate goal of combining several functions in a single package footprint still achievable, assembling and testing individual devices prior to final integration appears ideal. The issues associated with compound yield and test can be easily addressed by stacking separate packages. One example would be to package and test the ASIC separately from the memory functions in a two-section format typical of that illustrated in Figure 4-12.

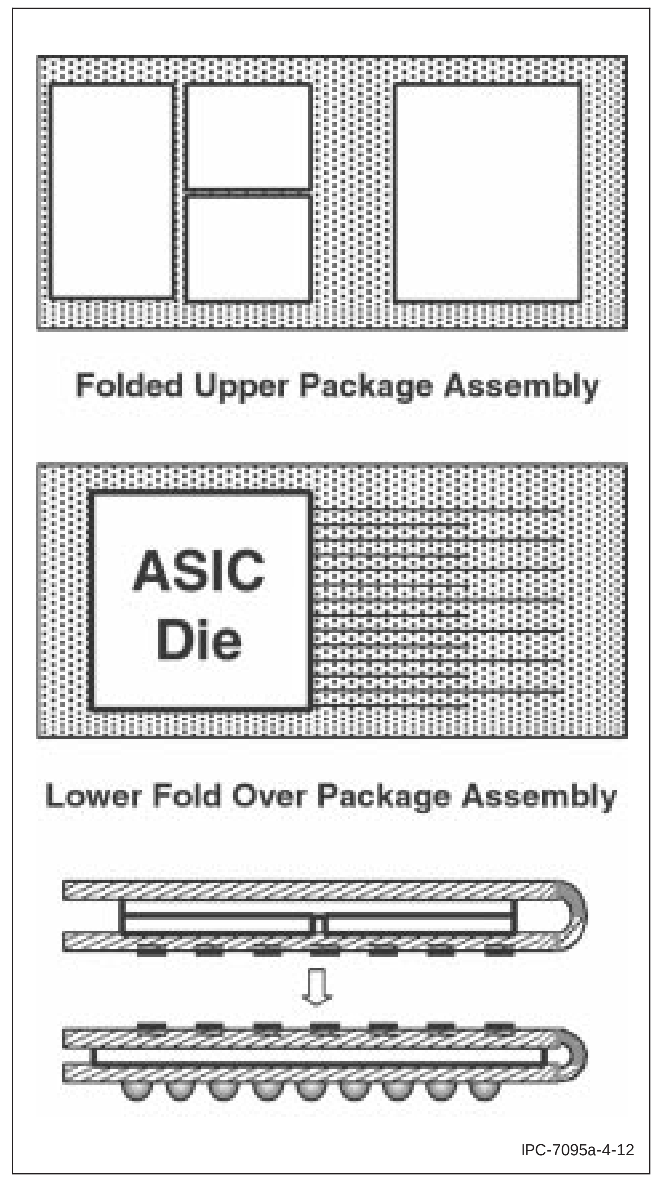


Figure 4-12 Folded and Stacked Multiple Die BGA Package

The lower and upper package assemblies with memory are processed and tested prior to the folding and joining operation. Through a process of folding and surface mount attachment, the two pretested sections become a single, high yielding multiple-function component. Furthermore, by providing a universal array pattern interface on the topside of the ASIC package, several variations of memory functions can be soldered directly onto the base package.

4.4.10 Benefits of Multiple Die Packaging The primary benefit in multiple die packaging is the dramatic increase in component density. The size and weight of the product is likely to be reduced and functionality enhanced. The functional enhancement is achieved through the integration of several device types. Other benefits include decreased circuit board complexity, improved product quality through higher reliability and reduced risk in getting the product to market. With multiple sourcing of already proven and mature die, time to market and cost of ownership can be minimized. The task of developing a multiple-die product are not without some obstacles. Some of the key issues are:

- Managing multiple vendors.
- Known good die test and burn-in methods.
- Die and wafer availability.
- Combining high and low yield devices. Overall product quality and reliability.

4.5 BGA Connectors

4.5.1 Assembly Considerations for BGA Connectors Several items need to be addressed concerning the placement and soldering of BGA connectors to a PCB substrate. Some BGA connector designs do not lend themselves to a vacuum pick-up using standard SMT nozzles. In this case, two options are available:

1. Mechanical chuck pick-up using a custom nozzle.
2. Design the BGA connector with a cap or other temporary surface so a standard vacuum nozzle can be used.

Both options can be successful in production, and the best option is highly dependent on the connector design. Depending on the connector material, reflow profiles have to be examined and compared to the T_g temperature of the connector material. When the temperature of the connector increases beyond the T_g point, the connector will tend to either bow toward the board (‘‘flatten out’’) or bow away from the board (‘‘warp’’). The actual behavior is a function of the connector geometry, connector material, and the surface tension of the connector balls to the substrate. Also included in this analysis are the connector coplanarity requirements for successful soldering. The material properties behavior during reflow) and the overall connector size will dictate the connector ball coplanarity requirements. Typically, BGA connector’s coplanarity requirements are stricter than standard BGA packaged IC components due to their increased size.

4.5.2 Material Considerations for BGA Connectors The BGA connector shown in Figure 4-13 is designed to provide a relatively low profile horizontal or parallel interface between two circuit assemblies. The material engineered for this application has been developed to withstand the reflow soldering temperatures associated with surface

mount assembly and furnish a reliable interconnect in the varying environmental conditions typical of the products end use.

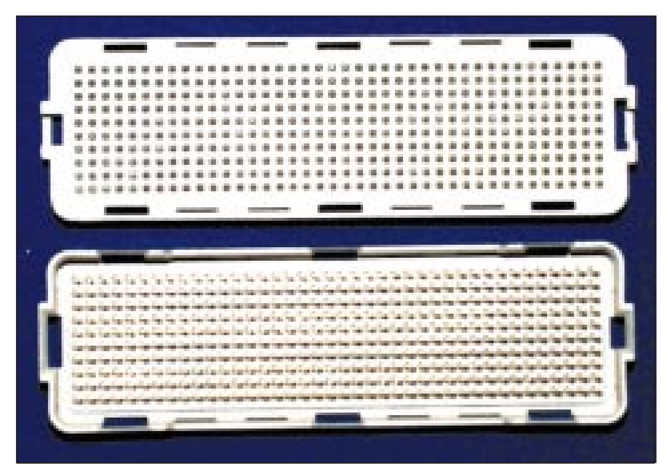


Figure 4-13 BGA Connector

It is important to understand the material properties of the connector system. During the life of the product, the circuit board assembly will undergo many varying thermal cycles. These thermal cycles will cause material expansion/contraction to the assembly components, including the BGA connector. Therefore, material selection for BGA connectors is significant due to the thermal interaction of the connector to the PCB substrate. Specifically, the BGA connector material's coefficient of thermal expansion (CTE) must be matched to the CTE of the PCB substrate material.

If there is a significant CTE mismatch between the BGA connector (typically a LCP material) and the PCB substrate (typically FR-4), the resulting thermal stresses on the solder joints could cause cracking and ultimately solder joint failure.

4.6 BGA Construction Materials

4.6.1 Types of Substrate Materials A number of different materials are used in the construction of BGAs. The material choice is predicated on a number of different factors including cost, use environment, reliability requirements, etc. The material choice is also dependent on the processes used in the manufacture of the BGA and the complexity of the design required to redistribute the chip I/O to area array format. Base materials are selected not only by their electrical characteristics, but also their mechanical properties. Most component manufacturers require that the material used to redistribute the I/Os meet a stress test identified in the JEDEC standard, JESD22, Test Method A102B. The test consists of an exposure in a pressure vessel for 168 hours. This severe, highly accelerated stress test (HAST) permits the use of only the most robust materials for the substrate interposer when HAST is required.

4.6.1.1 Bismaleimide Triazine-Glass (BT) Bismaleimide triazine resins used in combination with glass fabric reinforcements are a common choice for the fabrication of substrates used in BGA packages. The material is available from a number of sources and provides good thermal performance (based on a relatively high glass transition temperature). In addition the electrical properties of BT resin are acceptable for a great number of IC package applications.

4.6.1.2 Epoxy-Glass (FR-4) A fire retardant epoxy-glass laminate, can be used for a limited number of BGA package applications but the material is most commonly in the manufacture of printed circuits. High T_g FR-4 laminates (tetrafunctional, multifunctional) have been predominantly used in manufacturing multilayer circuit boards but the material may be considered for BGA packaging as well. Recent advances in the epoxy-resin materials have resulted in greatly improved high temperature performance and rivals BT in terms of glass transition temperature. Another advantage of using FR-4 resin systems for BGA construction is that they are matched in CTE to the circuit board onto which they are mounted.

4.6.1.3 Ceramic Ceramic is the term used for a general class of substrate based on alumina or aluminum oxide. The material is one of the first used for area array packaging in the form of pin grid arrays and was also the material first used in the construction of its earliest BGA packages. Ceramic substrates have higher thermal conductivity and using a cavity and lid format, can provide hermetic packaging capability. Ceramic does, however, have a number of limitations. For example, it is normally more expensive, more brittle, has a higher dielectric constant (which retards signal propagation speed) and has a coefficient of thermal expansion much lower than the typical circuit board structure onto which it is normally mounted. This last point is a major concern and can limit the overall package size and the need to maximize the ball contact size in order to achieve acceptable solder joint reliability of the assembled package.

4.6.1.4 Flexible (Nonreinforced) Base Films Flexible base films are an increasingly common choice for BGA construction. The most common base film for such constructions is polyimide. Polyimide has a number of attractive attributes, which make it a strong choice for BGA substrates. Among the positive attributes offered by polyimide films are very high temperature limits (~250°C) and relatively low dielectric constant (~3.5 versus ~4.5 for FR-4 and ~10.0 for ceramic). In addition, it is very thin and is much easier to produce the fine line circuit features more commonly required for high-density area array packages.

On the negative side, the main concern with nonreinforced or flexible materials has been their dimensional stability.

The reinforcement provides the physical characteristics that enhance CTE properties in the X-Y axis. The X and Y axis are the particular segments of the interconnecting product that affects the stress on the solder joints of the package when mounted onto the interconnecting product. In addition, polyimide film is generally more expensive than some of the other reinforced organic base materials and it is relatively hydroscopic. On the other-hand, because polyimide films are more flexible, the material will absorb rather than transfer physical stress.

4.6.2 Properties of Substrate Materials While there are numerous properties that are specified and measured, relative to substrate materials, only a few properties are considered key to the performance of the final BGA product.

4.6.2.1 Coefficient of Thermal Expansion (CTE) The coefficient of thermal expansion is a very important physical attribute of a BGA substrate. The CTE defines the rate of expansion of the material with increase in temperature. The importance is magnified when there are large differences in CTE between the BGA package and the circuit board structure to which it is mounted. When the CTE difference is large, excessive strain can be placed on the solder ball connections resulting in lower reliability of the assembled package.

4.6.2.2 Glass Transition Temperature (T_g) The glass transition temperature is the temperature at which the resin element of the laminate begins to soften and lose strength. It is also the point at which the resin begins to expand at a much higher rate (i.e., the material's CTE increases) primarily in the z-axis as the glass fabric controls the in-plane CTE.

4.6.2.3 Flexural Modulus Flexural modulus is important as a measure of the stiffness or rigidity of the substrate. The impact on the BGA is most commonly manifested in the degree of warpage. This in turn can significantly impact board assembly yield if warpage is excessive.

4.6.2.4 Dielectric Properties There are several metrics that are embraced under the general heading of dielectric properties. Dielectric constant, dissipation factor, dielectric withstanding voltage and surface insulation resistance are examples of such properties. These properties are important, moreover as computers and modules obtain processing speeds towards the 400 MHz level, signal speed and integrity become paramount. The high speed is mainly for the microprocessor. The interconnecting bus speed requirements are somewhat less; in the neighborhood of 100 MHz.

The need for greater performance capability will be apparent as systems designed to be run above 200 to 300 MHz, continue to use FR-4. As processing speeds continue to increase, it is necessary to lower the dielectric constant and also lower the dissipation factor of the material. The more advanced substrate material systems can provide robust solutions. For example, cyanate-ester provides signal transmission speeds of 114 cm/nsec compared to 100 cm/nsec for common FR-4 epoxy material. Lower dielectric constant (Dk) and lower dissipation factor (Df) must be considered when selecting advanced material technologies.

Lower dielectric constant (Dk) benefits include:

• Faster conductor signal speed.

• Thinner interconnects for the same conductor geometries.

Lower dissipation factor (Df) benefits include:

• Improved signal integrity with high frequencies.

• Less signal loss at high frequencies.

Table 4-7 shows the different characteristics for some of the materials used to fabricate substrates for BGA applications.

4.6.2.5 Moisture Absorption Moisture absorption of materials used for BGA construction is something of great concern. The ideal material will not retain any moisture. From a packaging perspective, the concern is predicated on the fact that moisture can be trapped in the laminate base. Entrapped moisture can expand and outgas explosively during assembly causing local delamination, degrading the reliability of the package.

4.6.2.6 Flatness Requirements Flatness requirements for BGA substrates must be maintained to assure that the components will not be excessively warped or bowed after package assembly. Such conditions could make testing and the assembly to the next level difficult. The package assembly process will ameliorate some of the effects once the die is attached, especially if the die is of substantial size relative to the package. The recommended flatness criteria for BGA packaging should not exceed 0.3%.

4.7 BGA Package Design Considerations In addition to the die design rules, the substrate designer must understand both thermal and electrical performance issues. BGA package designers must consider manufacturability issues as well: substrate fabrication, first and second level assembly yield and finished package reliability.

4.7.1 Power and Ground Planes In package power and ground distribution must be planned in advance. For some high-speed applications, entire circuit layers are required for power and ground distribution. Ground and voltage planes are also used when controlled impedance transmission lines are required. In addition, a quiet ground needs to be separated from a noisy ground where all the switching activity takes place. Some applications require several power supplies with different voltages for each part of the

Table 4-7 Typical Properties of Common Dielectric Materials

Property	Material					
	FR-4 (Epoxy E-Glass)	Multifunctional Epoxy	High Performance Epoxy	Bismaleimide Triazine/Epoxy	Polyimide	Cyanate Ester
Dielectric Constant (Neat Resin)	3.9	3.5	3.4	2.9	3.5 - 3.7	2.8
Electric Strength (x 10^3 (V/mm) [x 10^6 V/in]	39.4 [1.0]	51.2 [1.3]	70.9 [1.8]	47.2 [1.2]	70.9 [1.8]	65.0 [1.65]
Volume Resistivity (x 106 D-cm)	4.0	3.8	4.9	4.0	2.1	1.0
Water Absorption (wt%)	1.3	0.1	0.3	1.3	0.5	0.8
Dissipation Factor	0.022	0.019	0.012	0.015	0.01	0.004

chip. These planes should be distributed evenly on the BGA package substrate to minimize component warpage.

For applications requiring a solid power or ground plane, a minimum of a four-layer substrate is required. The four-layer substrates will also exhibit lower thermal resistance and higher power dissipation compared to two-layer packages. In thermally enhanced BGAs where a copper heat sink is incorporated inside the package, the heat sink is commonly used as a ground plane. By connecting ground lines through vias to the heatsink, the heatsink becomes an active current-carrying ground plane.

4.7.2 Signal Integrity There are three major BGA package design considerations that affect signal integrity.

1. Reflections due to discontinuation in the characteristic impedance lines.
2. Cross-talk between adjacent lines generated from the coupled noise between an active line and the quiet line.
3. Switching noise generated from multiple outputs switching simultaneously which is commonly known as ΔI noise or SSO noise. Multiple simultaneously switching outputs (SSOs) require the power and supply lines to have a lower effective inductance (L_{eff}):

$$\Delta I \text{ Noise} = L_{eff} \frac{di}{dt} \text{ in millivolts}$$

The effective inductance in a BGA package depends on the number and placement of power and ground pins in relation to the power and ground pads on the die. By proper pin assignments for power and ground pins and commercially available signal integrity tools, L_{eff} as well as the ΔI noise can be minimized.

4.7.3 Heat Spreader Incorporation Inside the Package A heat spreader may be incorporated inside the package when the chip power exceeds the maximum power dissipation that can be supported by package substrate. Due to lower functional conductivity of some laminate material, most of the heat generated by the IC is carried through the copper conductors, plated through-hole vias, and the solder balls. By furnishing a copper plane or section under the die mounting area, a heat spreader is incorporated into the package. It is important that the package design is as thermally balanced as possible to avoid excessive warpage during temperature changes. In ceramic-based BGA the heat spreading can be achieved by replacing the low conductivity alumina-based ceramic material by high conductivity copper-tungsten materials having a thermal expansion coefficient matched to alumina substrate materials.

4.8 BGA Package Acceptance Criteria and Shipping Format There are several issues related to the acceptance criteria for BGA packages. These include having a process control strategy during qualification and production where sampling plans are used to define the level of nonconformance.

The major issues are:

1. Voids in eutectic solder ball.
2. Ball size and shape.
3. Ball coplanarity.
4. Missing ball.
5. Module flatness/package bow.
6. Presence of contamination.
7. CSAM for delamination.

4.8.1 Missing Balls Missing or damaged ball contacts are not acceptable on incoming BGA components. Figure 4-14 provides an illustration of balls missing from the BGA package.

4.8.2 Voids in Solder Balls Voids in solder balls should be based on incoming acceptance criteria or post-assembly solder joint acceptance criteria. Voids typical of that shown in Figure 4-15 may or may not dissipate during board level assembly processing. Reliability of the solder joint may be compromised if a void is excessive due to the reduction of solder volume and surface bonding area. It will be necessary to establish an acceptable level of voiding so that the

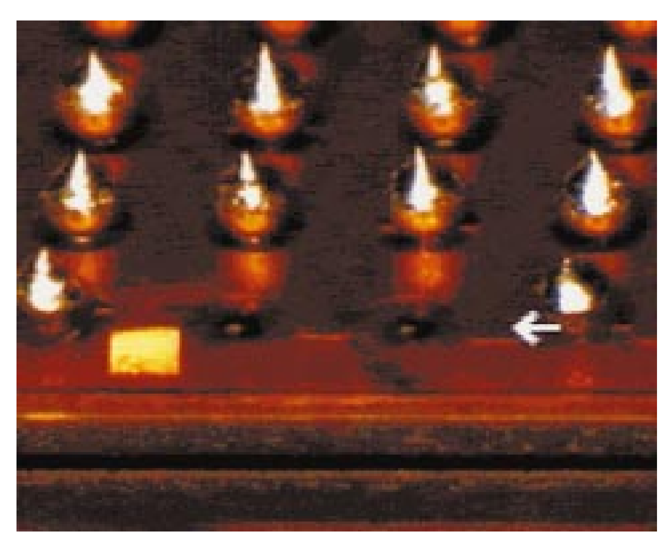


Figure 4-14 Example of Missing Balls on a BGA Component

product can meet customer expectations, has a useful working life and meets product reliability requirements. See 7.5.1 for post assembly process control criteria for solder ball voids.

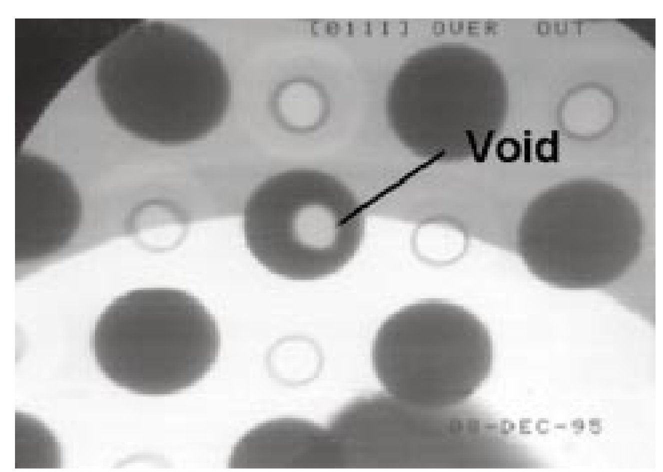
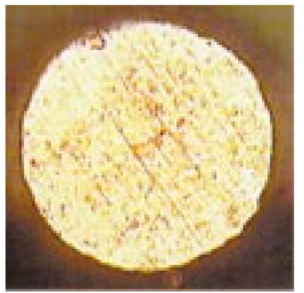
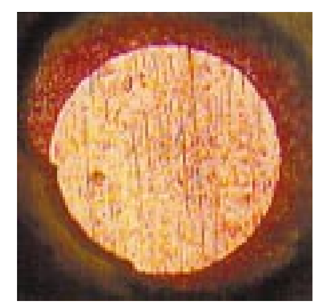


Figure 4-15 Example of Voids in Eutectic Solder Balls

4.8.3 Solder Ball Attach Integrity One of the factors the success of the BGA package depends upon is adequate solder ball attachment. The solder balls need to be attached within acceptable dimensional tolerances. Their height and width after attach need to be within specified and/or acceptable limits. Most important of all they need to form a proper metallurgical bond with the lands on the substrate. All solder balls need to see a temperature profile which ensures wetting necessary for optimum connection. If the joint does not wet (that is, it makes a cold solder joint) then the solder ball is not properly attached for necessary mechanical and electrical interconnect. Such balls may fall off during shipping, transportation and handling or may fail or act intermittently during electrical testing. Figure 4-16 shows the surfaces of the solder ball and the land, which did not wet to form a lasting metallurgical bond. The first picture shows the flattened bottom of a solder ball and the second picture shows the pad on an FBGA where it was supposed to be attached. Attach temperature did not reach high enough for the solder to flow and for the pad to wet for adequate adhesion. A small amount of force dislodged the solder ball from the pad.



Flattened bottom of a solder ball



Pad on an FBGA where it was supposed to be attached

Figure 4-16 Examples of Solder Ball/Land Surface Conditions

Solder ball attach integrity can be evaluated through solder ball shear. Manual and automated shearing and shear force recording instruments are available for the purpose (see IPC-9701). There is significant difference in the shear force of a wetted solder attach and cold solder attach. It should be noted that while using shear values to make decisions, the shear forces will decrease with decreasing attach area (land size) and will also depend upon the kind of solder constituting the solder ball. The shear interface should show the amount of wetting during reflow. For a good attach, there should be no unwetted areas.

4.8.4 Package Coplanarity Package Coplanarity is the result of all of the following factors:

1. Package Thickness, Pitch, and Thermal Requirements.
2. Substrate Design, Material, and Manufacturing Processes.
3. Number of Devices (Silicon)-Size and Thickness.
4. Number of Passives-Size and Thickness.
5. Assembly Materials and Manufacturing Processes.

The final Package Coplanarity is a very complex combination of these factors. A large percentage (~70%) of the package coplanarity is controlled by factors 1 and 2. The type of solder ball used will determine how much overall Package Coplanarity can be tolerated during the final Package to board assembly. This is why collapsing eutectic solder balls are the most popular because they can compensate for larger Package Coplanarity values.

The JEDEC design guidelines currently define the ball contact diameter (b) at its maximum diameter, as measured in a plane parallel to the seating plane, Datum C. The detail illustrated in Figure 4-17 defines the profile tolerance zone controlling coplanarity (ccc) and the limits for parallelism

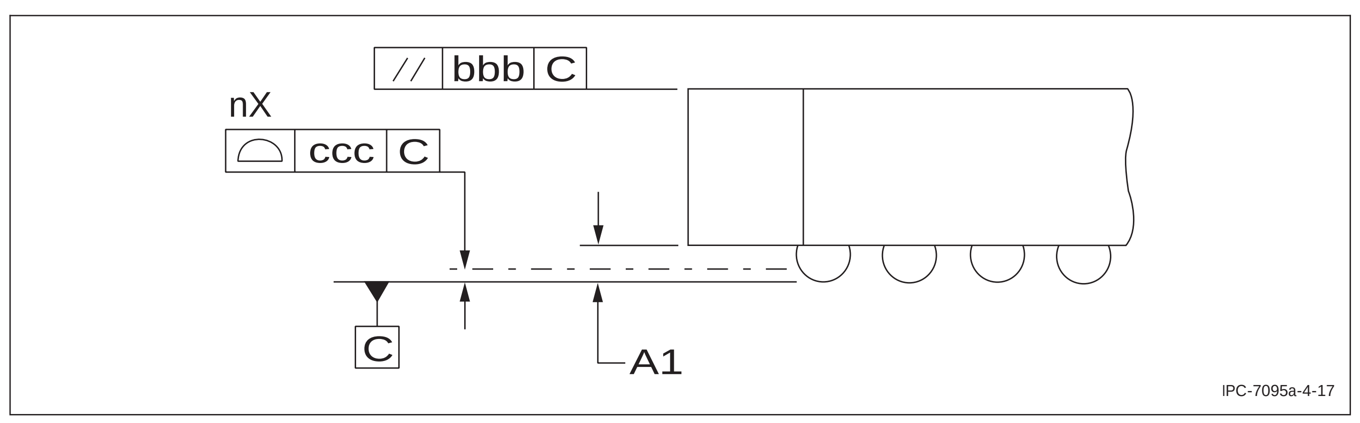


Figure 4-17 Establishing BGA Coplanarity Requirement

between the package top surface (bbb) and the seating plane (Datum C).

Package height is measured from top surface of the package to the seating plane (where the ball meets the mounting surface of the host PCB). It is important that the top surface of the package remains parallel to the seating plane, accommodating component handling in test, inspection and assembly. The bilateral tolerance zone (bbb) for parallelism references the top surface of the package with respect to Datum C, the seating plane.

4.8.4.1 Example for FBGA Coplanarity Tolerance limits for coplanarity varies slightly with the increase in ball diameter. The following shows the Controlled Coplanarity (ccc) per ball size:

0.30 mm ball = 0.08 mm (ccc)
0.40 mm ball = 0.10 mm (ccc)
0.50 mm ball = 0.12 mm (ccc)

The unilateral profile tolerance zone (ccc) extends upward from the seating plane. The lowest point of the ball contact must be within the tolerance zone. Each ball has a tolerance zone associated with diameter 'b' that is located on true position with respect to Datums A and B and is perpendicular to Datum C. The center of each ball must lie within the tolerance zone. The positional tolerance for the ball contact is defined with relationship to package outline Datums A, B and C. as illustrated in Figure 4-18.

The array of tolerance zones associated with the ball diameter (b), spaced on a basic pitch (e), controls the location of the balls. The design guideline allows the array to float with respect to the tolerance zone 'ddd' however, the centers of the balls must simultaneously lie within both tolerance zones. For more detail in measuring the BGA package see JEDEC JEP95, Section 4.17. (BGA Package Measuring and Methodology).

4.8.5 Moisture Sensitivity (Baking, Storage, Handling, Rebaking) Moisture sensitivity requirements are defined by J-STD-020 and J-STD-033. The J-STD-033 provides information on handling moisture sensitive components. Components are segregated into eight levels as shown in Table 4-8. These classes define how long a component can be left out on the production floor once removed from its sealed shipping bag. Parts exposed to ambient air for longer than the specified time must be rebaked prior to use, to drive out excess absorbed moisture.

Many BGA components are moisture sensitive; particular attention should be paid to TBGA and flip chip PBGA components. Ceramic BGA/CGA components are generally not moisture sensitive. It is recommended that BGAs meet at least Level 3 specifications. Level 5 and 6 parts are particularly undesirable from a manufacturing handling perspective, because they drive additional shop floor and component handling controls. In the case of Level 6 parts, bake-out ovens will be required. Bake-out may take between four hours and 48 hours at 125°C or five days to 68 days at 40°C depending on package thickness and size. In order to remove moisture from BGA components a recommended bake cycle should be established.

It should be noted that the higher reflow temperatures required for lead free solders may require a more rigorous moisture removal bake cycle. However, the J-STD-020 requires a shorter time in which the package is permitted to absorb the moisture.

4.8.6 Shipping Medium (Tape and Reel, Trays, Tubes) As with all SMT components, BGA parts should be packaged in ESD packaging which meets the requirements of the appropriate standards or specifications. BGA components should be available in JEDEC approved matrix trays able to withstand multiple bake cycles, as many BGAs are moisture sensitive. See 4.8.5 for required bake temperatures and times for the different classes of moisture sensitive components.

It may be preferable to procure high volume parts, e.g., SRAM or DRAM devices, in tape and reel for faster assembly cycle times. Component size and moisture sensitivity may dictate that tape and reel is not applicable for some BGAs. Tape widths up to 56 mm are available, and a

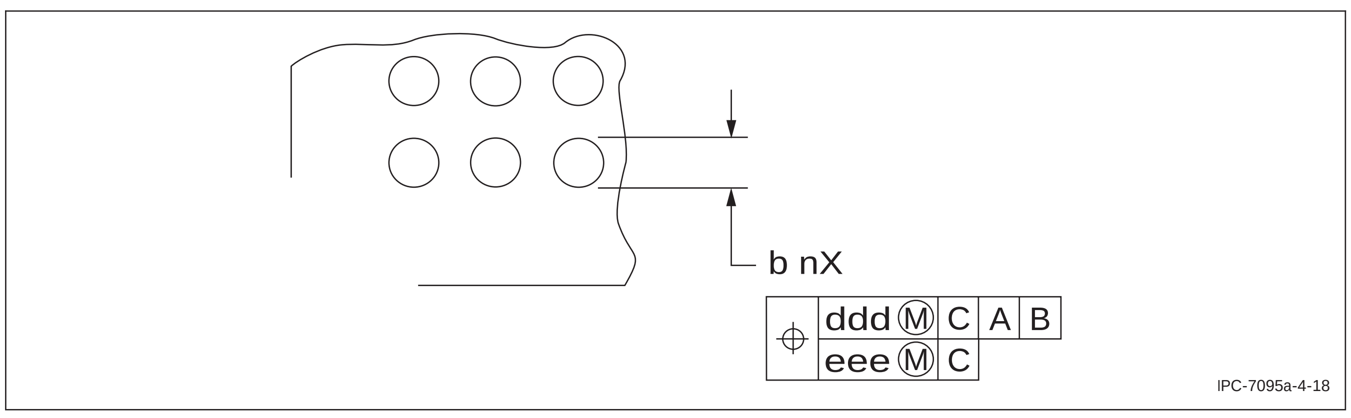


Figure 4-18 Ball Contact Positional Tolerance

Table 4-8 Moisture Classification Level and Floor Life

Level	Floor life (out of bag) at factory ambient ≤30°C/60% RH or as stated
1	Unlimited at ≤30°C/85% RH
2	1 year
2a	4 weeks
3	168 hours
4	72 hours
5	48 hours
5a	24 hours
6	Mandatory bake before use. After bake, must be reflowed within the time limit specified on the label

tape ''leader'' of at least 200 mm should be provided. Caution must be used when baking parts in tape and reel, as this type of packaging is usually restricted to lower bake temperatures than matrix trays.

5 PCBS AND OTHER MOUNTING STRUCTURES

There are a number of alternative mounting structures available to serve as substrates for electronic assemblies. They employ a wide range of materials and have a wide range of physical properties. The choice is normally made based on cost/performance needs of the finished product.

5.1 Types of Mounting Structures Following is an examination of some of the more commonly used mounting structure substrates.

5.1.1 Organic Resin Systems Organic substrates are the most commonly used in the construction of electronic interconnection structures. There is a well-established world wide manufacturing base for this type of product. As a result of the large manufacturing base, this type of interconnection structure is the lowest cost among the competing technologies. Organic materials have intrinsic beneficial electrical properties. Most notable is a relatively low dielectric constant on average which can be made much lower by the proper choice of resin and reinforcement.

5.1.2 Inorganic Structures Inorganic substrates are an alternative to the organic substrates. They have some significant benefits not easily obtained with organic substrates. Chief among these advantages is excellent thermal properties. Like organic structures there are a number of possible choices available, ceramic, silicon, and enameled metals. The dielectric properties of these materials tend to be higher than organic based materials and they are generally more prone to breakage. Finally because of the more limited vendor base these structures are normally more expensive.

5.1.3 Layering (Multilayer, Sequential or Build-Up) Multilayer interconnection structures are commonly required for today's high performance electronics. There are several approaches to creating this type of product. The traditional multilayer is created by printing and etching thin layers of copper clad substrates and laminating them into a monolithic structure which can be drilled and plated so as to make connection between the layers where required.

More recently, alternative structures have been developed to address the routing difficulties associated with BGAs. These structures employ new approaches to creating multilayer structures, variously referred to as build-up multilayers, sequential multilayers and co-laminated multilayers. A key feature of these structures is their use of very small vias or microvias as they have come to be commonly known. A typical microvia has a capture land (where the via starts) and a smaller target land (where the via ends). A conceptual drawing of some types of buildup multilayers is provided in Figure 5-1. The following are examples of different buildup constructions:

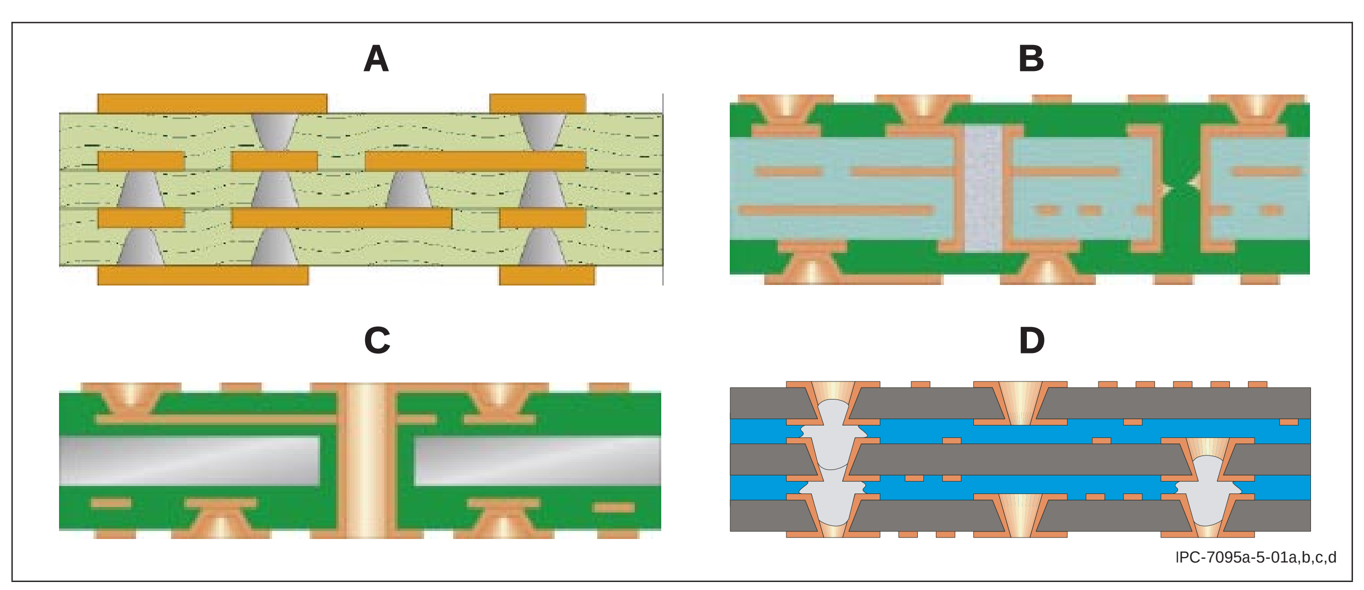


Figure 5-1 Examples of Different Build-Up Constructions

A. Piercing post co-laminated structure.

B. Sequentially built-up multilayer.

C. Passive substrate with external microvia layers interposer.

D. Filled via sequentially co-laminated substrate.

5.2 Properties of Mounting Structures

5.2.1 Resin Systems

5.2.1.1 Epoxy There are a number of different resin systems that can be used to create a printed wiring substrate. Epoxy is among the most commonly used resin systems for PCBs. It offers a good blend of physical, electrical and processing properties at reasonable cost. The general properties are provided in Table 5-1. Higher temperature capability epoxy resin systems are being developed and available at a cost premium.

5.2.1.2 Polyimide Polyimide offers the highest operating temperature among resin systems in use today. It has been a favorite for military applications where the potential for board rework and repair in the field is anticipated. Polyimide offers a real potential to reduce damage to the board when uncontrolled soldering irons are used to remove or replace a component. The general properties are provided in Table 5-1.

5.2.1.3 Bismaleimide Triazine Bismaleimide triazine or BT resin is the most popular choice for the construction of BGA packages because of its combined advantages of high temperature capability at reasonable cost. The general properties are provided in Table 5-1.

5.2.2 Reinforcements Reinforcements provide the dimensional stability and the bulk of the mechanical properties of the organic substrate laminate. Following are some of the more commonly used reinforcements.

5.2.2.1 Glass Cloth Glass cloths are the most commonly used reinforcement for PCB substrates. They are widely available and are processed with relative ease. The cloths are available in a number of different thicknesses and chemical make-ups. E type glass is the most commonly used glass cloth for printed circuit substrates.

5.2.2.2 Glass Felt Glass felt or nonwoven glass mat is most commonly used in combination with fluoroplastic resins.

5.2.2.3 Aramid Cloth Aramid cloth has been used to reinforce certain laminates. It has a negative CTE in the X and Y direction, which helps to offset the in-plane CTE of the resin. As a result laminates made from this material can match approximately the CTE of ceramic. A drawback of the material is a high Z axis CTE which can fracture nearby resin, leaving micro-cracks along the surface of the fibers.

5.2.2.4 Aramid Paper Aramid papers are being effectively used in a number of multilayer applications. They have most of the benefits of the aramid cloth with more process latitude. Because the material is organic, it has the added advantage of bring easily processed by either laser or plasma for making holes.

5.2.3 Thermal Expansion Thermal expansion is usually characterized in terms of changes to the x-y plane, which is controlled primarily by the reinforcement of the material. Thermal expansion also occurs in the z-axis at a rate significantly larger than in the x-y plane, particularly at temperatures above the T_g.

Table 5-1 shows the conditions for various reinforced resin types. All thermal expansion is measured in parts/million/change in temperature (°C).

Table 5-1 Environmental Properties of Common Dielectric Materials

Environmental Property	Material					
	FR-4 (Epoxy E-glass)	Multi-Functional Epoxy	High Performance Epoxy	Bismaleimide Triazine/ Epoxy	Polyimide	Cyanate Ester
Thermal Expansion xy-plane (ppm/°C)	16 -19	14 - 18	14 - 18	~15	8 - 18	~15
Thermal Expansion z-axis below T_g[3] (ppm/°C)	50 - 85	44 - 80	~44	~70	35 - 70	~81
Glass Transition Temp. T_g (°C)	110 - 140	130 -160	165 - 190	175 - 200	220 - 280	180 - 260
Flexural Modulus (x 10^{10}Pa) [x 10^6 psi] Fill[1]	1.86	1.86	1.93	2.07	2.69	2.07
Warp[2]	1.20	2.07	2.20	2.41	2.89	2.20
Tensile Strength (x 10^8 Pa) [x 10^4 psi] Fill[1]	4.13	4.13	4.13	3.93	4.82	3.45
Warp[2]	4.82	4.48	5.24	4.27	5.51	4.13
Water Absorption (wt%)	1.3	0.1	0.3	1.3	0.5	0.8

1. Fill - yarns that are woven in a crosswise direction of the fabric.
2. Warp (cloth) - yarns that are woven in the lengthwise direction of the fabric.
3. Z-axis expansion above T_g can be as much as four times greater. For FR-4 it is 240-390 ppm. Contact supplier for specific values of the other materials.

5.2.4 Glass Transition Temperature Glass transition temperature is that property of the material where the reinforcement and the resin systems deviate from their existing linear coefficient of thermal expansion and take on a new characteristic. This usually occurs when the resin system exceeds its cured polymer state. It is usually an expansion in the z-axis of the material and that the temperature stated expands at a faster rate, although still linear (mm/mm of thickness).

Table 5-1 shows some of the characteristics of the conditions for glass transition temperature of various material types.

5.2.5 Moisture Absorption Most organic materials are hygroscopic and can pick up moisture relatively rapidly. This moisture is recognized in the form of water absorption and changes the characteristics in the material, both in its dimensional configuration, as well as its weight. An easy manner in which to acknowledge that the material has absorbed moisture is to note the increase in weight due to the exposure to moisture conditions. Table 5-1 shows the water absorption rate by weight for the various materials highlighted in this section.

5.3 Surface Finishes The surface finish of the PCB may need to perform any of the following functions: solderability protection, conductive surface for contacts/switches, wire bonding surface, and solder joint interface. Although BGAs are the focus of this document, the other components and assembly operations of the PCB must be taken into consideration when choosing the most appropriate surface finish. There is no single surface finish that will be ''best'' for all applications. Some of the most commonly used surface finishes are described in more detail in the sections below: hot air solder leveling (HASL), organic surface protection (OSP), immersion tin, and noble coatings (including electroless nickel/immersion gold, electrolytic nickel/electroplated gold and immersion/silver).

Some of the application features that must be considered in selection of a suitable surface finish are given in Table 5-2.

5.3.1 Hot Air Solder Leveling The current predominant surface finish is hot air leveling (HASL) where solder is dipped in molten solder after the final copper plating process. In this process the board is either dipped vertically or horizontally in the solder bath at about 260°C and excess solder is blown away with hot air.

The key problem with HASL process is that solder thickness varies widely from 0.75 µm to 35 µm. It is generally believed that the lower thickness is not acceptable because the very thin layer of solder is completely transformed into copper-tin intermetallic, which has very poor solderability. However, studies [Ref: 9] on the solderability evaluation of printed circuit boards with HASL and other protective coatings indicated that soldering performance as indicated by visual examination showed absolutely no correlation to the solder thickness or solder coverage on the lands observed in cross-sections. As a result, acceptance criteria for the solderability of printed circuit boards should include or be entirely based on functional testing of sample boards.

The wide variation seen in solder thickness in HASL also adds to the coplanarity of boards and components. In addition, the uneven surface compounds the paste-printing

Table 5-2 Key Attributes for Various Board Surface Finishes

Characteristics	Hasl	OSP	Electroless NI/Immersion AU	Electrolytic Ni/ Electroplated AU	Immersion Silver	Immersion Tin
Shelf life proper handling	1 Year	6 Months	> 1 Year	< 1 Year	6 Months	6 Months
Handling/contact with soldering surfaces	Should be avoided	Must be avoided	Should be avoided	Should be avoided	Must be avoided	Must be avoided
SMT land surface topology	Inconsistent planar surface	Flat	Flat	Flat	Flat	Flat
Multiple (4) soldering cycles	Good	Fair to good, better with thick coatings	Fair to good	Fair to good	Fair to good	Fair to good
No clean flux use	No concerns	PTH/via fill concerns	No concerns	No concerns	No concerns	No concerns
Warpage concern on ≤1.0 mm thick PCBs	Yes	No	No	No	No	No
Solder joint reliability	Good	Good	BGA "black pad" and brittle solder joint concerns	Gold embrittlement concerns	Good	Good
Card edge contacts	Additional plating operation	Additional plating operation	Additional plating operation	Additional plating operation	Additional plating operation	Additional plating operation
Wire bonding	No	No	No	Yes	No	No
Test point probing	Good	Poor, unless solder applied during assembly	Good	Good	Good	Good
Exposed copper after assembly	No	Yes	No	No	No	No
Switches/Contacts	No	No	Yes	Yes	Yes	No
Waste treatment and safety in PCB fabrication	Poor	Good	Fair	Fair	Good	Good
Surface finish thickness control	Thickness control concerns	Good	Good	Gold thickness control concerns	Good	Good
Total coating thickness/ µm*	2.0 - 8.0	0.15 min. [no max.]	Au 0.08 min [0.08 - 0.13] Ni 3.0 - 6.0	Au 0.13 - 0.75 Ni 1.25 - 7.5	0.05 - 0.5 typical	0.65 minimum
Cost	1	1 (thick coatings)	1.1 - 1.3	1.2 - 1.5	1	1

*Thickness measured on a 1.6 x 1.6 mm land.

problem because it gets more difficult to achieve good gasketing while printing. Lack of gasketing means leakage of paste underneath the stencil and hence either frequent cleaning (lower throughput) or increased potential for bridging (lower yield). If this was not enough, wide spread use of PCMCIA (personal computer memory card international association) cards, which are about 0.5 mm in thickness, means that HASL cannot be used as this causes boards to warp like potato chips.

5.3.2 Organic Surface Protection With wide spread use of ball grid array (BGA) and finer and finer pitch devices, the need for flatter board surfaces is becoming more critical. Hence the popularity of alternative surface finishes in general and organic solderability preservative (OSP) in particular is increasing.

OSP is an anti-tarnish coating of an organic compound (benzimidazole-based compound) over copper surface to prevent oxidation. It is a water based organic compound that selectively bonds with copper to provide an organometallic layer that protects the copper. Various chemistries of OSPs are available. Some common ones are benzotriazol, imidazol and benzimidazol. They keep the copper surface solderable by preventing it from oxidation or tarnish. It is applied either by dipping the board in an OSP bath or by spray. Either method works well as long as the process is controlled to achieve uniform OSP coating. The coating thickness can be either very thin (100Å) or relatively thick 0.2 to 0.5 µm (2000Å to 5000Å). Please note that 25 µm equals 1 mil or 1000 micro-inches. The thicker coatings are much preferred over the thinner coatings especially if you need multiple reflow cycles and longer wait (in days) between soldering of each side.

The OSP surface has many advantages. Most important of all, it avoids the key problem of HASL by keeping the

board surface flat. It is also lead free and therefore may be considered more environmentally friendly. By providing good gasketing, it also reduces solder paste printing related defects and hence provides better overall yield.

Since the OSP coated surface essentially looks like copper (OSP coating is transparent), any paste misprint is very easily spotted because of color contrast. Alcohol, if used for washing off the misprinted paste, will also wash off coatings and hence increase the risk of oxidation of the copper. However, such boards can be recoated if necessary. Washing the board should be performed using a lint free damp cloth.

There are also some potential process incompatibilities with OSPs. For example, if paste or flux does not cover all land surfaces during soldering, there may be insufficient hole filling in wave soldering and dewetted appearance in reflow soldering (on the edges and corners of surface mount lands). This is why it is important for flux to get into the PTH during wave soldering to achieve topside fillet. In the SMT process the paste must cover the entire land surface to avoid dewetted appearance at the land edges. However such defects are cosmetic only. The joints are perfectly all right. As a matter of fact in some cases the pull strength of OSP joints have been found to be higher than HASL joints.

Examples of some other OSP issues to be kept in mind would be potential incompatibility with no-clean flux and terpene based solvents, solderability concerns when subjected to multiple thermal cycles during reflow, wave and hand soldering and bed of nail testing. Also, one of the key issues with OSP is the handling of the board. OSP boards should be handled only by their edges.

The most widely used surface finishes are HASL and OSP. However, noble metal coatings such as gold and palladium are also used. None of the finishes are ideal for each application. The selection of a specific coating should be based on the specific application and familiarity with the technical and business issues related to that technology.

5.3.3 Noble Platings/Coatings Noble platings are becoming more commonly used as PCB surface finishes. Both electroless nickel/immersion gold and electrolytic nickel/electroplated gold finishes provide good shelf life, a flat soldering surface for SMT, and a good electrical probe surface for ICT. They both maintain a solderable surface through multiple reflow operations, and don't degrade due to handling. The presence of nickel plating strengthens the through-hole barrels during multiple reflow cycles and rework of through-hole components. Noble plating finishes typically cost more than OSP finishes, and are either comparable or more expensive than HASL, depending on the complexity of the PCB. If it is desired to mix multiple board finishes on a single board, for example Ni/Au in some areas and OSP in others, this can be difficult and expensive to achieve.

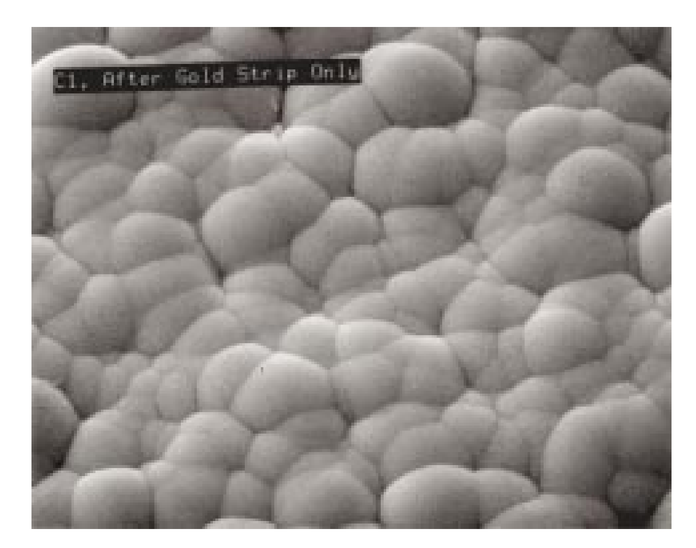
Application of electroless nickel/immersion gold can be performed using a variety of chemistries, which may lead to different finished results depending on the chemistry used. Also, the chemistry and process may be incompatible with some solder masks.

Phosphorous or Boron containing reducing agents are used for the reduction of the electroless nickel during the deposition process. Phosphorous or Boron is thus incorporated in the nickel deposit. The level of these co-deposited elements should be controlled within the specified process limit. Variation of phosphorous or boron level, outside the specified process limits, may have adverse effects on the solderability of the finish.

Many companies have used Electroless nickel/immersion gold as a surface finish successfully. However, when BGAs are used with the electroless nickel/immersion gold finish the results, at times, can be unpredictable. Two failure modes have occurred in recent years. The first failure mode is a non-wetting or dewetting condition referred to as ''black pad.'' The second failure mode is an interfacial fracture that is associated with mechanical stress.

Results from industry consortia and studies by individual companies suggest that ''black pad'' is caused by an aggressive attack (hyperactive corrosion) of the electroless Ni plating during the immersion Au plating process. The gold ions from the plating solution attract electrons from the metallic nickel surface as they plate out as the gold metal; in return a nickel ion is released to the bath. Due to certain microstructure features, such as grain boundaries and the electrochemistry involved, the exchange does not always occur locally, i.e., the gold can be deposited to one feature or area and the nickel ion released from a different feature or area. The possible consequence of this process is that selected nickel features become attacked leaving behind a rough and phosphorous rich layer that forms a weak bond with solder. The affected solder joints do not form a robust mechanical bond with the PWB and as a result the solder joints fail with a relatively small applied force; revealing lands with little or no solder left on them. The exposed nickel surface on the land is smooth with an appearance varying from grey to black in color, which is where the term ''black pad'' comes from (see Figures 5-2 and 5-3). SEM analysis shows a distinctive nickel nodular structure similar to ''mud cracks.'' EDX indicates high amounts of phosphorous and nickel and low amounts of tin. Corrosion marks and a phosphorous rich layer are observed from a polished cross-section.

Occurrence of the ''black pad'' condition does not appear to be sufficiently common to advise against use of electroless nickel/immersion gold as a surface finish. Assemblers



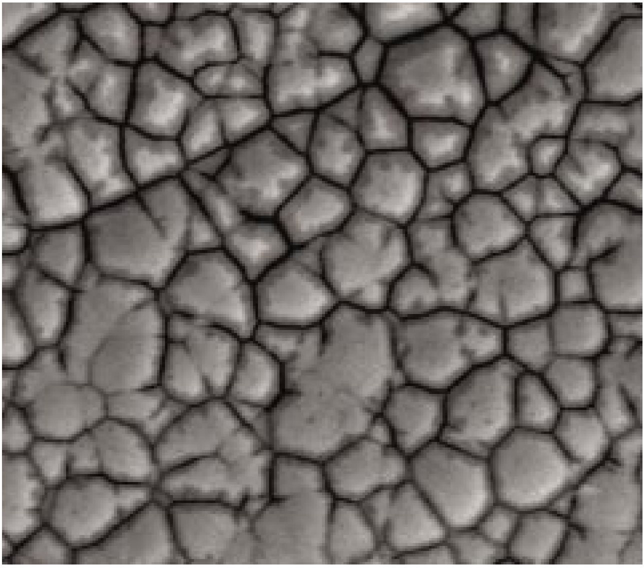


Figure 5-2 Typical Mud Crack Appearance of Black Pad Surface

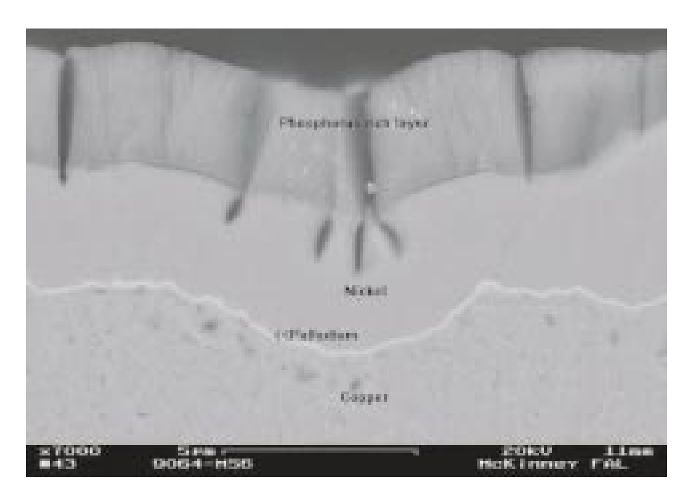


Figure 5-3 A Large Region of Severe Black Pad with Corrosion Spikes Protruding into Nickel Rich Layer Through Phosphorus Rich Layer Underneath Immersion Gold Surface

using PWBs with this finish should be aware of the potential problem, learn to recognize it, and take corrective action.

Recent analysis indicates that the interfacial fracture of the solder joint happens between the nickel surface and the nickel-tin intermetallic layer under a high level of both applied strain and strain rate even if hyperactive corrosion does not take place. Failures have occurred under a variety of laboratory testing conditions including bending, mechanical shock, and thermal cycling. Data indicates that increasing the strain rate shifts the failure mode to an interfacial fracture of the solder joint. Therefore interfacial failure may occur under a reduced strain if the strain rate is high enough. Currently there is no industry specification that quantitatively assesses the mechanical strength of assembled BGA components on any surface finish.

Another version is the electrolytic nickel/electroplated gold surface finish. This plating is similar however it results in a different grain structure from electroless nickel/immersion gold, and does not exhibit the 'black pad' joint cracking phenomenon.

Electrolytic nickel/electroplated gold is applied after pattern plating and most often before solder mask, and therefore carries some risk of surface contamination. Solder mask applied over electrolytic nickel/electroplated gold exhibits lower solder mask adhesion than other surface finishes. This can create problems during assembly of BGAs, and especially during rework. If the solder mask dams covering the traces between BGA lands and vias peel off, solder will flow from the BGA lands into the vias and cause insufficient or open solder joints.

Another concern is that it can be difficult to control the gold thickness across the board. The gold may be too thin (for example in areas with dense circuitry) or the gold may be too thick (for example in isolated circuits). This latter situation may lead to gold embrittlement due to excessive gold (>3%) in the solder joints.

In situations where large boards (>250 x 250 mm) are used with large BGAs (>25 x 25 mm) it may be a good idea to increase PWB thickness to at least 2 mm to minimize board bending and flexing. This will reduce or eliminate interfacial failures due to mechanical stress that is caused by bending and flexing of the PWB.

The industry continues to search for alternative surface finishes that can overcome the disadvantages associated with the HASL, OSP, and ENIG finishes. Some of the most promising new surface finishes are immersion silver and immersion tin. Both immersion silver and immersion tin are deposited on the board surface using the immersion method of metal deposition.

Immersion Silver is a metallic solderability preservative. It can be permanent, becoming an integral part of the

assembled board, or sacrificial, preventing copper oxidation and preserving solderability through the assembly process. Immersion silver is also a good surface for contact probe testing.

Immersion Tin is a metallic solderability preservative that is sacrificial, preventing copper oxidation and preserving solderability through the assembly process. Due to the higher contact resistance of tin it is not as good as immersion silver for contact probe testing.

Due to the lack of a ''perfect'' surface finish the search continues for a better surface finish solution. Although early results look good for some of the immersing surface finishes, immersion silver in particular, more testing and industry experience is required before conclusions can be drawn regarding BGA solder joint reliability and new surface finishes.

5.4 Solder Mask The solder mask is a polymer. However, unlike the laminate it is not a composite but a homogeneous material. As the name suggests, this material is used to mask off the outer areas of the board where solder is not required to prevent bridging between conductors. In the past not all boards required a solder mask because the conductors and lands were spaced quite far apart. The solder bridges between adjacent conductors during wave soldering were not critical. But with the advent of fine lines and spaces, the use of a solder mask has become almost mandatory for boards that are going to be wave soldered. On a full SMT board where no wave soldering is required, tenting or plugging of via holes is done to assist drawing a vacuum on some ICT testers. Also, the application of solder mask to block or plug a via allows closer spacing between a via and the adjacent conductor lines.

The two broad categories of solder masks are permanent and temporary. Temporary solder masks are washable or peelable. They are used during wave soldering to prevent filling of holes that must be kept open for the installation after soldering of such leaded items as unsealed parts that might not withstand the cleaning or soldering environments. The temporary masks that can be peeled off are also used to mask off gold lands, which must not be soldered.

Washable masks are more convenient than peelable masks because they come off in the cleaning operation after wave soldering and do not need an extra step to remove them. The aqueous washable solder masks require an aqueous cleaning system, and the solvent washable masks must be washed in a solvent cleaning system.

5.4.1 Wet Vs. Dry Film Solder Masks Permanent solder masks come in dry film and wet film. Dry film masks can have an aqueous or a solvent base. In both cases, the mask starts out as a polymer film, which is applied to the board by vacuum lamination.

Wet film solder masks, as the name implies, are liquid or pastelike. They include photoimageable and wet screenable solder masks. The latter are differentiated by the method of cure. Some wet screenable solder masks can be cured by UV light and some can be cured thermally in convection or IR ovens. UV masks do not provide as good adhesion as thermal masks but require only seconds to cure as opposed to 30-60 minutes for thermal cure.

Each of the solder mask categories has advantages and disadvantages. They are inexpensive and highly durable. Being liquid, they flow between conductors and prevent the formation of air pockets. There is no trim waste, and the thickness of the mask can be controlled for each design. Since the wet film solder masks are screened on (a mechanical process), they are difficult to register and have a tendency to skip over conductors, especially on fine line boards. They also tend to bleed onto the lands and surface mount lands during cure. Wet screenable masks are difficult to use on boards with fine lines and spaces (<200 µm), and they are also vulnerable to voids, bubbles and pin holes. The use of screenable mask has been on decline as photoimageable solder masks have gained in popularity.

The wet film solder mask cannot successfully tent via holes. Generally these materials fill one side of the vias partially, which can prevent bridging but is ineffective in sealing holes to prevent vacuum leakage during testing. The degree of fill needs some control in order to develop a plug that prevents chemistry from going through the via.

Partially filled vias trap process chemicals and are difficult to clean. Dry film solder masks have some advantages over their wet screen counterparts. The former provide very accurate registration, which is critical in preventing solder bridging or bleeding on fine line boards, as well as sharper resolution. Tenting of via holes is also superior with dry film solder masks because they are never in a liquid state and do not drip into the via during vacuum lamination. However some problems arise when trying to laminate a semisolid dry film over an uneven board surface with conductors and lands. Any warping and twisting of the board will compound the problem, possibly causing air pockets underneath the dry film near conductors.

The curing of a dry film solder mask is extremely critical for achieving a reliable coating. Insufficient cure can cause cleaning problems because of diminished resistance to chemical attack by fluxes or cleaning solutions. Overcure results in a brittle mask, which can crack easily under thermal stress.

Most dry film solder masks are not resistant to thermal shock. Cracks develop in the cured masks within 100 cycles of thermal shock cycling from +100°C to -40°C. This can be a problem especially in SMOBC boards because of exposed copper conductors. However, there are

some solder masks, commercially available, that resist cracking during thermal shock.

Dry film masks are more costly than the wet film variety, and the vendor base is limited. Moreover, the application process for dry film solder masks is very difficult to control. Not many film thicknesses are commercially available, and this can limit flexibility and increase cost. Typically, most dry film solder masks are quite thick, 75 µm to 100 µm. Trim waste also adds to cost.

Nonwetting of surface mount boards containing wave soldered chip components sometimes occurs because of the greatest thickness. In addition, the thicker mask surrounding the small vias may prevent them from filling with solder during wave soldering (crater effect).

The thicker masks can cause problems in reflow soldering as well. For example, a dry film mask applied between the lands of passive surface mount devices can cause tombstoning (standing up on edge) during reflow soldering because of the rocking effect of the mask. For this reason dry film solder mask should not be used between the lands of chip resistors and capacitors or in assemblies that have components glued to the bottom side for wave soldering.

5.4.2 Photoimageable Solder Masks Photoimageable solder masks combine the advantages of dry film and wet solder masks. Dry film is also a photoimageable mask. In this section, however, our discussion is focused on wet film photoimageable masks, which provide accurate registration, are easy to apply, encapsulate the circuit lines totally, have excellent durability, and are cheaper than dry film [Ref: 2].

Photoimageable masks can be either screened on or applied by a process called curtain-coating, in which the board is passed at high speed through a curtain or waterfall of solder mask.

The photoimageable mask may contain solvent along with photopolymer liquid. If the solvent is added in the mask, the liquid mask is screened on, solvent is dried off in an oven, and then the mask is exposed to UV light by off-contact or on-contact methods. (If no solvents are used, the liquid is 100% reactive to UV light.) The off-contact method requires a collimated light system to minimize diffraction and scatter in liquid. This makes the system very expensive. The on-contact approach needs no collimated UV light source, and the system is relatively cheaper. Photoimageable solder masks can tent only very small via holes. Most photoimageable wet film masks will not even tent 0.35 mm via holes because it is difficult to cure polymer in via holes. If tenting is required, dry film is needed because only dry film can tent via holes effectively.

5.4.3 Registration Registration between individual boards becomes critical for any surface mount application. This is especially true when the board is made in a panel array format to assist the assembly process and throughput characteristics. Board manufacturers inherently build printed boards in a manufacturing panel format; assemblers also want to take advantage of the multiple board array format when they complete their assembly.

The positioning of individual boards on any panel is usually at the discretion of the board manufacturer. The manufacturer optimizes the use of the material in the panel and the tolerance conditions that can be achieved with the material used to build a particular board. It is a well known fact that organic material moves, thus board manufacturers, based on the knowledge of this movement, adjusts the phototool to compensate for material stretch or shrinkage depending on the circuit and the board size.

Assembly companies build their stencils based on the step-and-repeat of an individual board into an array subpanel. It is critical to understand the exact layout used by the board manufacturer in providing the relationships of a land pattern for a BGA on one board, compared with the land pattern on a sister board in the same array. Inconsistent arrangement of the assembly array can make misprints in the stenciling of solder paste onto the panel for surface mount assembly.

In the past it has been a practice to rotate some boards on a panel in order to facilitate the maximum use of the material. This practice can be quite dangerous in that the ‘‘work-and-turn’’ creates some array panels with a different shrinkage factor than others. Figure 5-4 shows an example where two array panels were laid out on the manufacturing panel in a horizontal position, and one laid out in a vertical position to accommodate material usage. The shrink factor on the horizontal version of the material based on the glass cloth reinforcement would be relatively different than that of the array panel position in a vertical plane. Manufacturers are cautioned to communicate the complexity related to using the work-and-turn process before proceeding into the manufacturing steps.

5.4.4 Via Filling Via filling, capping, flooding tenting and plugging (conductive or nonconductive), are processes which cover or fill via holes with solder mask. Via filling is done usually on boards that use both reflow soldering and wave soldering. Via filling is recommended under certain conditions, for example boards that expose vias under BGAs that are wave soldered. When a board with BGAs on the first side is processed through wave soldering, a large amount of heat can transfer from the vias. This is very significant in BGAs where via hole density can be very high. The BGA’s joints can reflow again in the wave. Reflow without flux could lead to cold solder and open joint.

Via plugging may be useful on wave solder boards that are directly connected to BGA lands or directly connected by trace to BGA land. A recommended clearance for BGA is to cap or tent all vias that are less than 1.0 mm from the

Figure 5-4 Work and Turn Panel Layout

BGA lands (see Figure 5-5). Vias could be outside the BGA perimeter or under the BGA. Via capping is the preferred method since tenting reliability is dependent on the finished hole size.

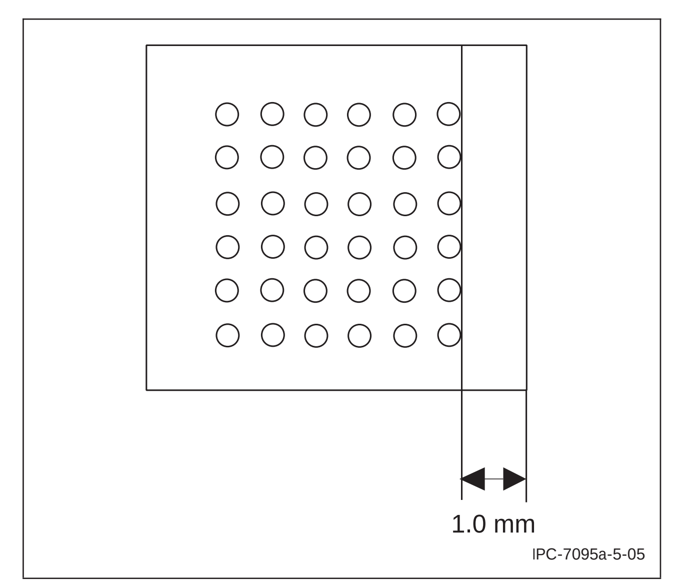


Figure 5-5 Distance from Tented Land Clearance

The following definitions apply to any via filling operation. There are four basic concepts which include:

- ***Tented Via –*** A via covered with dry film soldermask; the via has no fill. When tenting from both sides there may be issues with air entrapment and expansion during mass soldering. When tenting on one side there may be issues with chemical entrapment during the assembly process, especially when using aggressive flux.
- ***Flooded Via –*** A via that is flooded with LPI soldermask; the via is partially filled or the walls are coated with soldermask.
- ***Capped Via –*** A secondary operation that applies soldermask on one or both sides of the via; the via is partially filled, usually with a space between the two caps. When capping from both sides there may be issues with air entrapment and expansion during mass soldering.
- ***Plugged Via –*** An additional operation which is done prior to solder mask application; the via is filled with a conductive or nonconductive material.

Via plugging is frequently used in conjunction with BGA vias to prevent solder flow to the BGA solder joints when

wave soldering is used. Table 5-3 shows the relationship between via filling and the surface finish conditions.

Table 5-3 Via Filling to Surface Finish Process Evaluation

Surface Finish	Tenting	Flooding	Capping	Plugging
HASL	Okay	Okay	Okay	Okay
OSP	Okay	Not Recommended	Okay	Okay
ENIG	Okay	Okay	Okay	Okay
ImAg	Okay	Not Recommended	Okay	Okay
ImSn	Okay	Not Recommended	Okay	Okay

As a general rule, via flooding and capping should be done after surface finish application. On OSP and ImAg via capping must be done after the surface finish is applied because the harsh chemicals that are used to clean the copper surface can become trapped around the via cap. These trapped chemicals can damage the via wall resulting in open vias. Applying the via caps after the surface finish has been applied can degrade the surface finish (OSP, ImAg, ImSn) due to the thermal exposure that is necessary to cure the via cap material.

There are eight different methods of via plugging/capping identified in IPC standardization. These are shown in Figure 5-6. It is important to realize that the choice of tented, plugged and filled vias for via protection can have direct impacts to the subsequent assembly processes.

Besides the eight identified methods, Table 5-4 compares the pros and cons of commonly available options offered by board fabricators. The preference of plugging methods and options presented depends on the capabilities of both the fabricators and the assemblers. To avoid complication during assembly, it is imperative to understand the trade-off between these options.

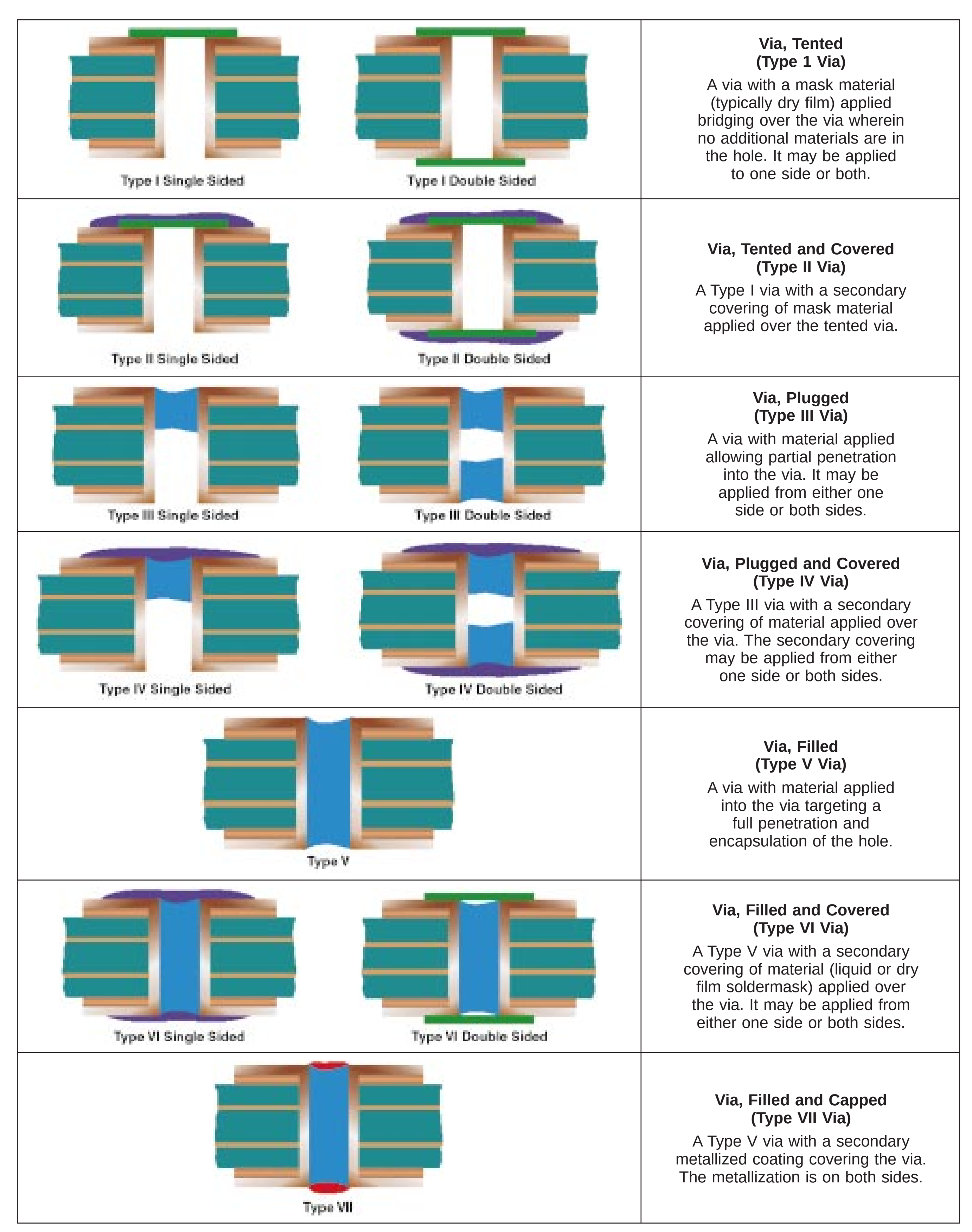
For PCB with HASL finish, solder coating prevents external chemical attacks and increases overall wall thickness ofvia barrel. However, for vias solder coated before plugging, the solder coating will reflow and turn molten during second sided reflow. The plugging material can become loose as a result. In some cases when there is excessive solder coating thickness or solder entrapped within via during fabrication, solder can potentially explode or drain to the remaining openings (see Figure 5-7). This is especially problematic when plugging is applied only to the bottom side of the BGA.

5.5 Thermal Structure Incorporation (e.g., Metal Core Boards) When structural, thermal, or electrical requirements dictate, a constraining core or metal core is added to the organic substrate to make the new structure. It is recommended that the board configuration be symmetrical about the center of the core. It can be asymmetrical where there are a different number of layers to either side of the core, however plated-through holes going through the entire stack may be less reliable due to the differences in expansion on either side of the metal or constraining core. There are advantages in an asymmetrical design in that the electrical properties and function are separated from the mechanical, or heat dissipation, function. The drawbacks are that, due to the differences in coefficient of thermal expansion of the board and the core material, the completed board may distort during assembly soldering/reflow operations, or while in system use due to temperature changes.

Some compensation can be achieved by having additional copper planes added to the back of the interconnection product. The extra copper plane increases the expansion coefficient slightly, but a positive effect is that it enhances thermal conductivity.

Table 5-4 Via Fill Options

	Top	Bottom	Top & bottom	No plug
Pros				
Increase rework robustness	Yes	Yes	Yes	No
Reduce secondary reflow risk at wave	Yes	Yes	Yes	No
Prevent solder drain	Yes	Yes	Yes	No
Cons				
Secondary Fab process	Yes	Yes	Yes	No
Component side height profile restriction	less than 50 µm above solder mask	No	less than 50 µm above solder mask	No
Contaminant concern	Yes (if exposed to wave solder directly, there is a potential of flux entrapment)	No	Yes (Contaminants entrapped within the via can be difficult to detect)	No
Plug integrity concern	Yes	Yes	Yes	No



Type I Single Sided Type I Double Sided	**Via, Tented (Type 1 Via)** A via with a mask material (typically dry film) applied bridging over the via wherein no additional materials are in the hole. It may be applied to one side or both.
Type II Single Sided Type II Double Sided	**Via, Tented and Covered (Type II Via)** A Type I via with a secondary covering of mask material applied over the tented via.
Type III Single Sided Type III Double Sided	**Via, Plugged (Type III Via)** A via with material applied allowing partial penetration into the via. It may be applied from either one side or both sides.
Type IV Single Sided Type IV Double Sided	**Via, Plugged and Covered (Type IV Via)** A Type III via with a secondary covering of material applied over the via. The secondary covering may be applied from either one side or both sides.
Type V	**Via, Filled (Type V Via)** A via with material applied into the via targeting a full penetration and encapsulation of the hole.
Type VI Single Sided Type VI Double Sided	**Via, Filled and Covered (Type VI Via)** A Type V via with a secondary covering of material (liquid or dry film soldermask) applied over the via. It may be applied from either one side or both sides.
Type VII	**Via, Filled and Capped (Type VII Via)** A Type V via with a secondary metallized coating covering the via. The metallization is on both sides.

Figure 5-6 Via Plug Methods

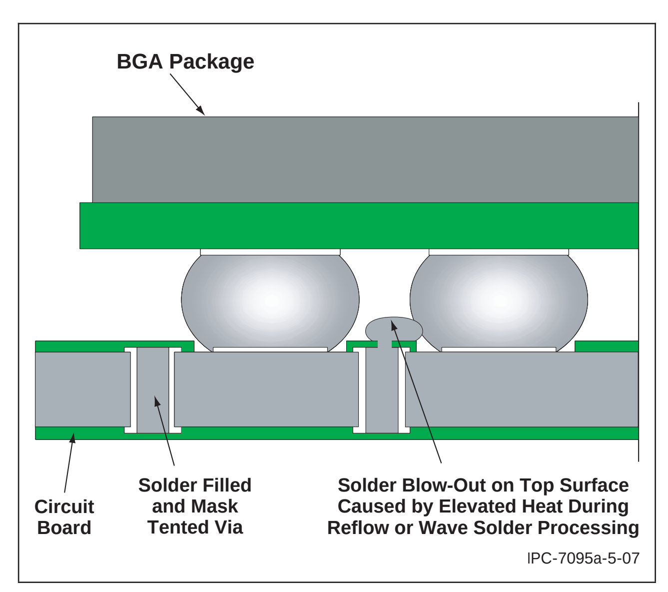


Figure 5-7 Solder Filled and Tented Via Blow-Out

5.5.1 Lamination Sequences More desirable construction is one where layers are symmetrical about the core of the board. In this fashion, individual multilayers are produced separately in their own laminating sequence. A four layer board might be manufactured which has vias through the entire four layers, which is then duplicated for either side of the core.

To achieve constraint in the useful range, the combined thickness of the core in the multilayer should be approximately 25% of the board thickness. Constraining core board is more often used because the core layers may be imaged, etched, and connected to the plated-through hole. The thicker center core must be machined. Better thermal cycle survival is exhibited by two constraining cores in the board than one.

Another configuration is to have a special constraining core board made by bonding a multilayer board to each side of a thick metal core after each of the boards have been completed. The composite board is then sequentially drilled, plated, and etched to form plated-through hole connections between the two boards. Coupons should be provided to test the integrity of the composite structure.

5.5.2 Heat Transfer Pathway Metal core boards add significantly to the thermal mass of the assembly. This may force the preheating soldering process to be operated at abnormally high limits. These designs should be thoroughly evaluated under production conditions prior to release. Laminate ruptures and discoloration and grainier textured solder are typical effects that have been observed. The heat transfer path between components and the planes are usually accomplished through either direct contact with the plane or through thermal vias positioned under the component and connected to the thermal core or plane in its position.

6 PRINTED CIRCUIT ASSEMBLY DESIGN CONSIDERATION

6.1 Component Placement and Clearances It is recommended that sufficient clearance (3 to 5 mm) be provided around BGAs to facilitate rework. The high-end clearances are recommended, especially for CBGA when using a step stencil to deposit solder paste and using hot air for rework. However, if using diode laser systems for rework the spacing can be reduced to 0.5 mm to 1.00 mm since laser does not impact adjacent components.

6.1.1 Pick and Place Requirements An advantage of BGA packages over other advanced, high-pin count packages (fine pitch, TAB, PGA, etc.) is the ability to be placed using existing surface mount placement equipment. No special placement and clearance requirements are needed for the component pick and place operation.

6.1.2 Repair/Rework Requirements Repair/rework of BGA components is a major driver for component spacing requirements. A typical BGA rework method requires five steps: (1) heating the solder joints to reflow temperatures for package removal, (2) removal and clean-up of solder on the BGA land pattern, (3) application of new solder paste or flux, (4) placement of the new BGA package, and (5) heating the solder joints to reflow temperatures for assembly of the BGA component to the circuit board. A keepout area may be needed for each of these steps. Rework equipment manufacturers can provide specific details regarding necessary keepout areas. General rules are outlined below.

Nearly all hot air methods use a nozzle system that fits down over and/or around the BGA package to heat the solder joints for removal and reflow. A component keepout area of 2.5 mm away from the outer edge of the oven nozzle is suggested. Including the nozzle size results in a 3.8 mm clearance from the component body. This spacing around the BGA provides room for the nozzle and reduces the risk of heating solder joints of adjacent components above the reflow temperature. When using laser for rework, the keepout area can be reduced to under 1 mm.

After a BGA package has been removed from the board during repair, the solder lands must be cleaned and new solder paste or flux applied before a new component can be placed. If the solder paste or flux is dispensed using manual methods or if solder paste is applied using an automated dispensing system, then there are no special component keepout areas required. However, many repair systems use a miniaturized stencil and squeegee to manually apply solder paste. In general, a minimum of 3 mm component keepout (i.e., the nominal distance between the body of the component and the body of the neighboring component) is needed so that both the nozzle clearance requirement and the mini-stencil requirement can be met. The existence of a

high profile neighboring component may require the minimum distance to be much larger than the stated minimum value.

6.1.3 Global Placement There are no special global placement requirements for BGA packages. However, it is recommended that they not be placed near the board centerlines. This reduces the potential of coplanarity problems associated with the board warping during reflow. In addition, BGA packages should not be placed next to large through-hole components as these can significantly increase the localized stiffness.

6.1.4 Alignment Legends (Silkscreen, Copper Features, Pin 1 Identifier) Alignment features printed on the circuit board are recommended for BGA packages to verify component alignment before and after reflow. BGA packages, especially PBGA, will self-align during reflow, even when placed up to 50% off the lands. As a result, any misalignments are generally one land diameter length or more off.

Alignment features will help verify that the component placement is sufficiently accurate with visual inspection. Silkscreen and copper are the two main materials used for alignment legends. Silkscreen is the most visible material, but requires the additional process step during board manufacturing. Copper alignment legends are created at the same time all other copper features are created and, therefore, leads to more accurate placement.

In many instances, legend is used by equipment or individuals to evaluate the alignment of the BGA during the placement operation. For peripheral leaded components, the fiducial has been standardized so that placement equipment can adjust the movement of the placement head accordingly and improve the final component positioning.

Fiducials are normally put at opposite corners to allow adjustment for the theta angle. This technique has been incorporated into many placement tools and equipments. The use of fiducials may not provide the most obvious condition for human inspection, however most inspectors can approximate that the package is properly centered between two fiducials that are known as local fiducials in order to accommodate their position. In some instances, companies have used angle brackets in place of the fiducials to assist the human eye in making this judgment, however the camera for placement equipment is not familiar with that configuration thus the practice is not the most conducive for proper assembly (see Figure 6-1).

Using silkscreen, the entire package can be outlined for easy visual alignment. Another alignment pattern commonly used is to mark just the corners of the BGA package. Corner marks should only be 0.8 mm long on each side. Copper can be used for corner marks, as it won't interfere with routing runs.

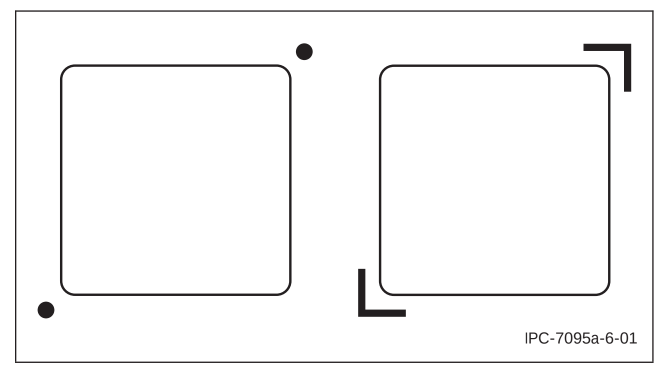


Figure 6-1 BGA Alignment Marks

(Optional: It is also possible to route runs around the corners of the BGA package and use them for alignment legends. This would require exposing the runs from solder mask so that the runs used for alignment are easily distinguished from other marks.)

All alignment legends should be offset 0.25 mm away from the outer edge of the BGA package. This gives sufficient clearance to view the features all around the BGA package. Pin #1 identifiers are required on BGA land patterns. This identifier can be a caret, dot, or other easily visible shape. The pin #1 identifier can be either silkscreen or copper and should be distinct enough so as not to be confused with any other markings around the land pattern.

6.2 Attachment Sites (Land Patterns and Vias)

6.2.1 Big Vs. Small Land and Impact on Routing The diameter of the solder land can affect both the reliability of the solder joints and also the routing of conductors. The land diameter is usually smaller than the ball diameter of the BGA. The land size reduction of 20 to 25% has been determined to provide reliable attachment criteria. The larger the lands, the less room for routing between lands. For example, a 1.27 mm pitch BGA package with 0.63 mm diameter solder lands will be able to fit two conductors between the lands using 125/125 µm conductors and spacing. If a 0.8 mm diameter solder land is used, only one conductor can fit between the solder lands using 125/125 µm conductors and spaces.

Tables 6-1 and 6-2 show the number of conductors that can be routed between lands for various land diameters and conductor/space widths.

The following equation can be used to determine the number of conductors that can be routed between lands depending on package pitch (P), solder land diameter (D), number of conductors between lands (n) and conductor/space width (x).

$$P - D \geq (2n + 1)x$$

A general rule is to design the solder land on the circuit board with the same diameter as the solder land on the plastic BGA substrate.

Table 6-1 Number of Conductors Between Solder Lands for 1.27 mm Pitch BGAs

Solder Land Diameter (micron)		750	700	625	500	400	350
Conductor Spacing Width (micron)	200	N/A	N/A	1	1	1	1
	150	1	1	1	2	2	2
	125	1	1	2	2	2	3
	100	2	2	2	3	3	4
	75	2	3	3	4	5	5

Table 6-2 Number of Conductors Between Solder Lands for 1.0 mm Pitch BGAs

Solder Land Diameter		625	500	400	350	300	250	200
Conductor Spacing Width (micron)	200	N/A	N/A	1	1	1	1	1
	150	N/A	1	1	1	1	2	2
	125	1	1	1	2	2	2	2
	100	1	2	2	2	2	3	3
	75	2	2	3	3	4	4	4

Solder land sizes for CBGA should be designed such that the stencil aperture will deposit a minimum of 0.08 cu mm of solder paste. This minimum requirement is necessary to ensure reliability of solder joint which comes from the melted solder paste deposit.

6.2.2 Solder Mask Vs. Metal Defined Land Design There are two basic types of solder lands used for BGA packages. These are nonsolder mask defined (NSMD) and solder mask defined (SMD). NSMD lands are copper defined as there is solder mask clearance around the lands, similar to most surface mount lands. SMD lands have solder mask overlapping the copper land (see Figure 6-2). Both land types have advantages and disadvantages.

6.2.2.1 Nonsolder Mask Defined Lands NSMD lands require a smaller diameter copper land and, therefore, have more metal-to-metal spacing for routing and vias. Copper dimensions can also be controlled better than solder mask dimensions, giving a more uniform surface finish, especially for HASL boards. The absence of solder mask around the solder land allows the solder to flow around the edges of the land, eliminating any areas of stress concentration. This makes the solder joint much wider, potentially giving it longer fatigue life, but lowers the stand off height.

6.2.2.2 Solder Mask Defined Lands Because of the overlapped solder mask, SMD lands require a larger diameter metal land to achieve the same sized land diameter as NSMD. The solder joint is narrower, but will have a higher standoff. The SMD lands adhere to the board more because of the larger surface area of copper and the overlapping solder mask. Although there are some advantages of SMD lands, the major disadvantage is that this approach is less

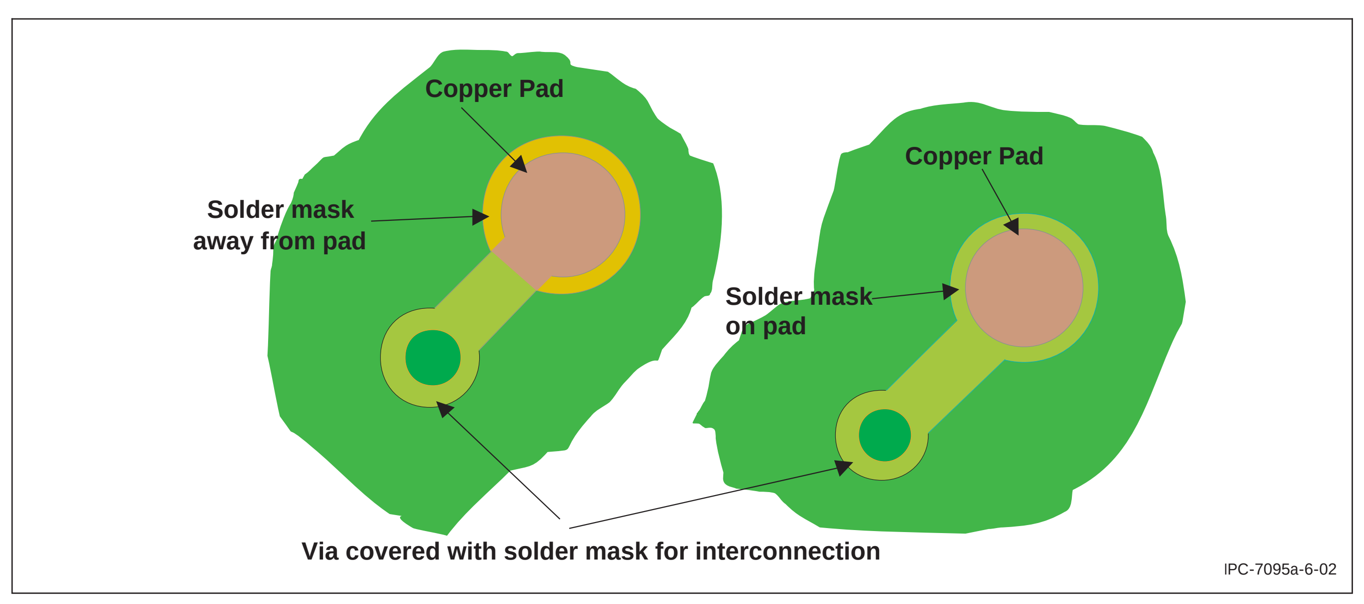


Figure 6-2 Solder Lands for BGA Components

reliable, decreasing the fatigue life by up to 70 percent when compared to NSMD lands. An area of high stress is created at the solder mask opening.

6.2.3 Conductor Width The conductor width can affect the routing of the BGA package. The wider the conductor, the less room between lands for placing runs. There is no maximum conductor width recommendation for SMD solder lands. However, the maximum conductor width connecting NSMD solder lands is 0.2 mm. Anything wider will have the effect of changing the solder land to an SMD type land at the location. For the same reasons, only one run should be joined to any NSMD solder land. To eliminate sharp corners, a fillet should be used where the conductor connects to the solder land.

6.2.4 Via Size and Location Vias can be placed between BGA solder lands on the land pattern. Via lands should be kept small enough to provide clearance between it and adjoining solder lands. The maximum via size that can be used depends upon the size and type (SMD vs. NSMD) of solder land used. However, it is recommended that the smallest standard via land/drill size be utilized for the board thickness. Vias with 0.6 mm lands and 0.35 mm drilled holes are common for 1.5 mm and 1.27 mm pitch BGAs, while 0.5 mm lands/0.25 mm drilled holes are used for 1.0 mm and 0.75 mm pitch packages.

To minimize the risk of solder bridging between standard sized vias and solder lands, vias can be either tented or have solder mask encroaching (overlapping) the via land.

Covering the via lands will also reduce the risk of narrow solder mask dams peeling off during BGA rework. See Figure 6-3 for examples of covered vias and narrow solder mask dams. Tented vias may not be reliable with some combinations of solder mask and surface finish. The solder mask opening on an encroached via should be just large enough to allow flux and other contaminants to escape during processing. Consult your board fabricator for capabilities when planning to tent or use encroached solder mask on vias.

Other options for vias on BGA land patterns include blind vias and micro vias. Blind vias can be created using a standard drill process, laser ablation, or photo defined through wet or dry (plasma) chemistry. The outer and inner layers are sequentially built and are then laminated together. Because the via penetrates only the outer layers, a smaller sized drill can be utilized. However, this option is generally a large cost adder. Blind vias can be placed between solder lands, but because of their smaller via lands, centering the via between the solder lands is not as critical.

Microvias are created in a secondary operation and penetrate the outer layers only. A standard micro via connects

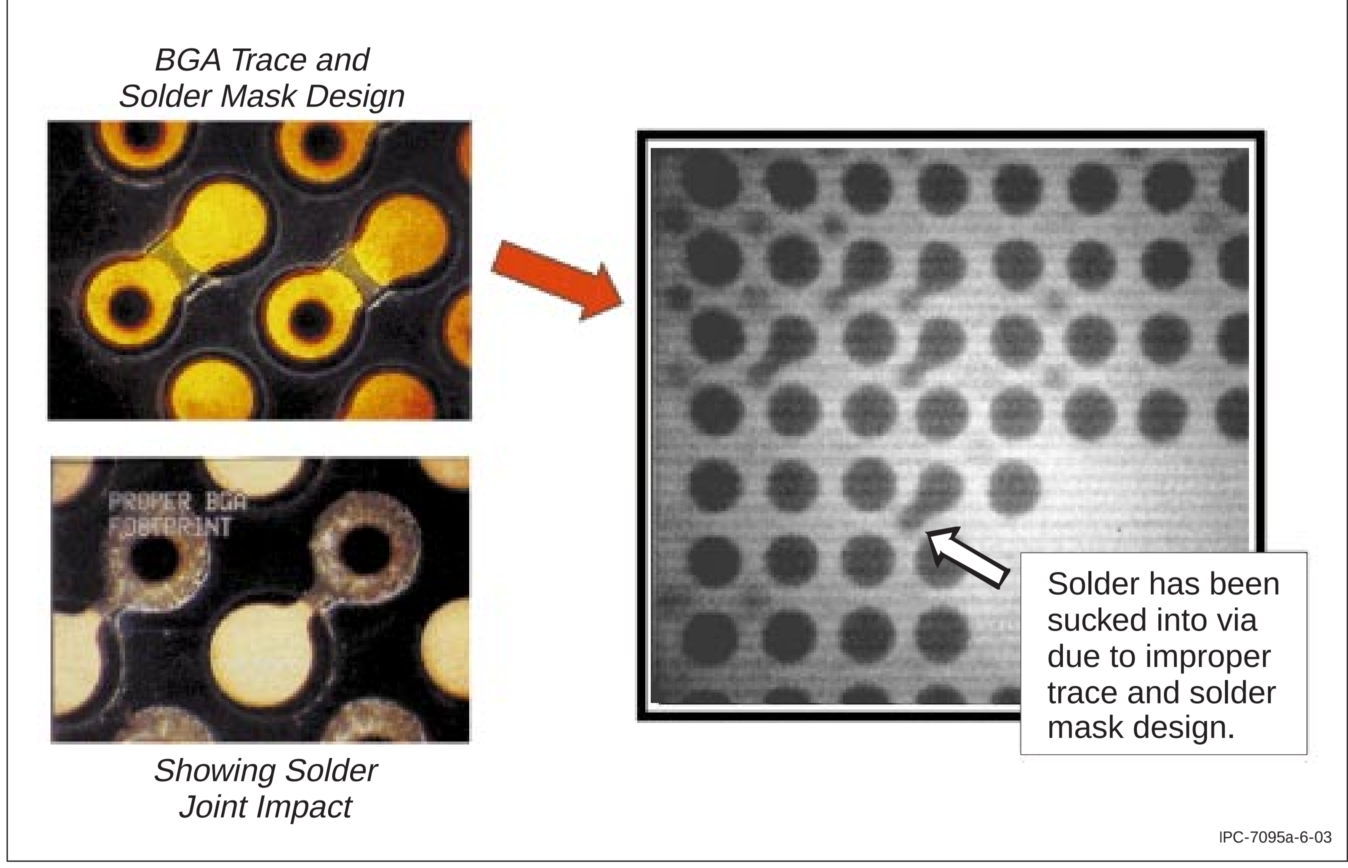


Figure 6-3 Good/Bad Solder Mask Design

layers 1 and 2 and/or n-1 and n. A typical micro via can have a 0.3 mm land with a 0.1 mm hole size. Because of this small size, the via can actually be placed in the center of the solder land with the only noticeable effect being a small dimple. By placing vias directly in the land, the space between BGA solder lands on the outer layers can be used exclusively for routing.

One should establish a liaison with a board manufacturer for options and rules before designing BGA land patterns with blind or micro vias.

6.3 Escape and Conductor Routing Strategies Unlike peripherally leaded packages, BGA solder joints are not all easily accessible on the top board layer. This is especially true for BGA packages with large, full grid arrays. Additional layers may be required to route the signals out from underneath the middle of these packages.

For example, a 1.27 mm pitch, 357-pin PBGA has a 19x19 full grid array without the corner solder balls. If 0.63 mm solder lands are used, this leaves only 0.63 mm between lands for routing conductors. This would permit only one 0.2 mm conductor between the lands, meaning that only the outer two rows (136 pins total) of the package could be routed out on the top layer. All other pins (221 total) would need to join to vias and then routed out through other signal layers. If 125 µm conductors/spacing is used, two conductors could be placed between lands so that the outer three rows of pins (192 pins total) could be routed out on the top layer, leaving the remaining pins (165 total) to be routed using vias.

To ease routing, power and ground pins can be placed in the center of the array pattern so that they can be connected directly to vias and not interfere with routing around the outer edges of the package.

Ball grid arrays can be square or can be rectangular. In a square array, the number of rows are equal to the number of columns. A 4x4 square array is shown in Figure 6-4.

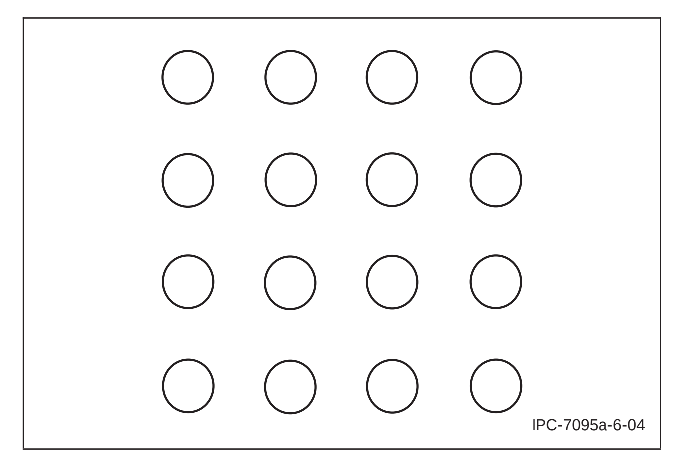


Figure 6-4 Square Array

In a rectangular array, the number of rows is not equal to the number of columns. A 4x5 rectangular array is shown in Figure 6-5.

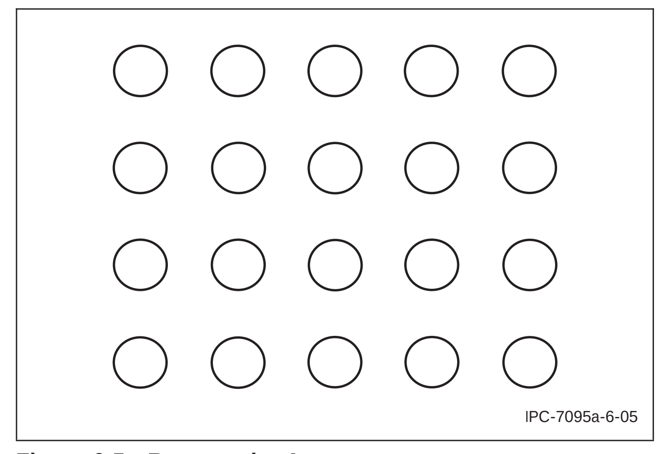


Figure 6-5 Rectangular Array

The arrays may be completely filled or certain portions of the array may be unfilled. A 4x5 rectangular array is shown in Figure 6-6 which has the one central column unused, blank, or depopulated.

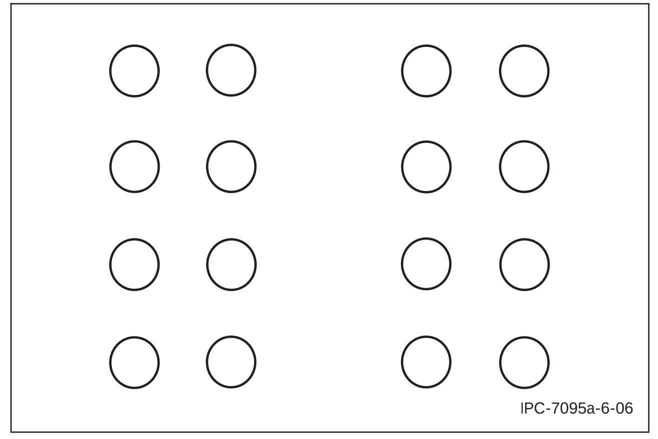


Figure 6-6 Depopulated Array

The 4x4 square array shown in Figure 6-7 has some balls missing, blank or depopulated.

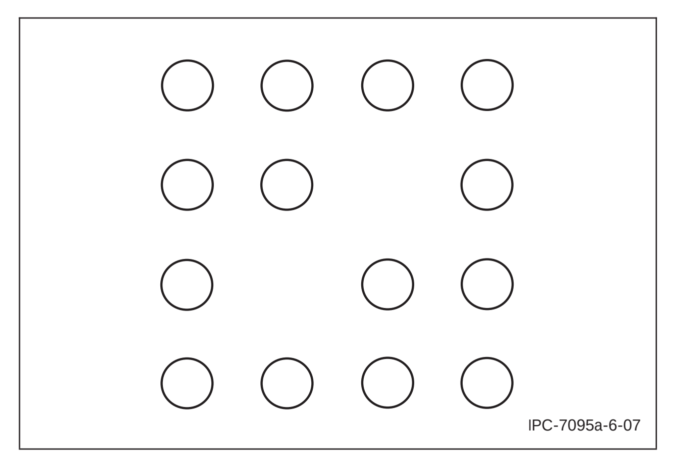


Figure 6-7 Square Array With Missing Balls

It is relatively trivial to fan out the conductors from the outlying balls to the periphery for interconnection to the outside world. But the solder balls inside the array have to be routed in between the outlying solder balls.

As the size of the array increases, more and more traces from the solder balls inside the array have to be routed in between the solder balls to connect to the outside world. It is important for the substrate designers to know how many conductors they may expect to accommodate in the spacings between the adjacent solder balls so that they may determine the widths of the conductors and the spacing between the conductors. This information will help to model the signal integrity to assure the success of their application.

The number of conductors per outlet, C, for a simple r x c array can be determined by substituting r and c in the following relationship with the number of rows and columns of the given array, and by substituting d with the number of depopulated sites in the array.

$$C \; \frac{[(r-2)(c-2)]-d}{2(r+c-2)}$$

In case the above equation provides a whole number for C, every array outlet between adjacent solder balls will need to accommodate C conductors. If C is a fractional number then some outlets will have to accommodate a number of conductors obtained by rounding down the value of C and others will have to accommodate a number of conductors obtained by rounding up the value of C. The fraction is the proportion of the lower and higher number of conductors per outlet.

The balls in an array can also be interspersed, as in a diagonal array. An example of a 5x5 interspersed array is shown in Figure 6-8.

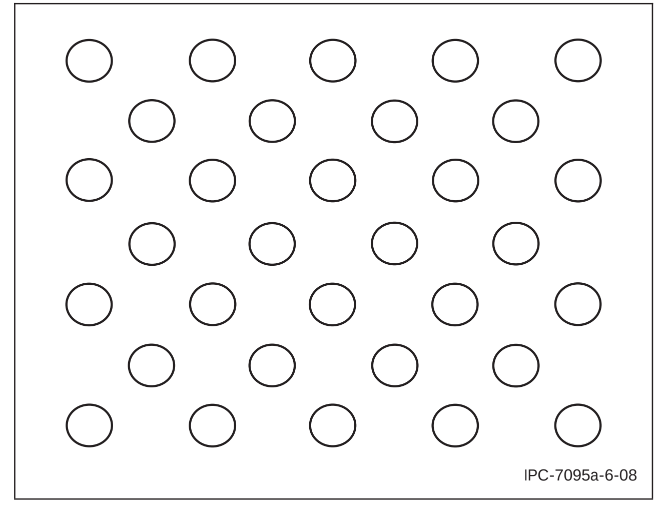


Figure 6-8 Interspersed Array

The following relationship can be used to determine the number of conductors per outlet for an interspersed array.

$$C = \frac{[(r-2)(c-2)+(r-1)(c-1)]-d}{2(r+c-2)}$$

If C turns out to be a fraction, then rounding it down will give the lower number of conductors to be accommodated between some adjacent balls, and rounding it up will provide the number of maximum conductors needed to be accommodated between other adjacent balls. The fraction gives the proportion of the two numbers.

The sizes of the solder land and via land also affect the routing ability of BGA packages. A 0.8 mm solder land on a 1.27 mm pitch leaves only 0.5 mm between solder lands for routing. In order to get two conductors between the solder lands, 100/100 µm conductors/spacing would need to be used. However, if a 0.6 mm solder land is used, two conductors can be routed between lands using 125/125 µm conductors/spacing.

Because of the small space between solder lands on finer pitch BGA (1.00 mm and less), smaller via lands and drill sizes are required. As the drill sizes get smaller, the maximum allowable board thickness also decreases. This may force board designers to use fewer layers or to decrease the dielectric thickness between layers.

If micro vias are used, this may force the outer two layers of the PCB to be signal layers.

6.3.1 Uncapped Via-in-Pad and Impact on Reliability Issue Via-in-pad (through-hole via, capped on bottom of the board) for BGA lands can cause voids in the BGA solder joints, which may impact reliability. Current data indicate that, for the standard 25 - 35 mm package with 0.75 mm balls, there is no reliability risk from voids. Accelerated aging tests have been performed and the failure rate was statistically equivalent to standard dog bone designs. It appears that void consistency is more important than void size with respect to joint reliability. An illustration of the problem is shown in Figures 6-9 and 6-10.

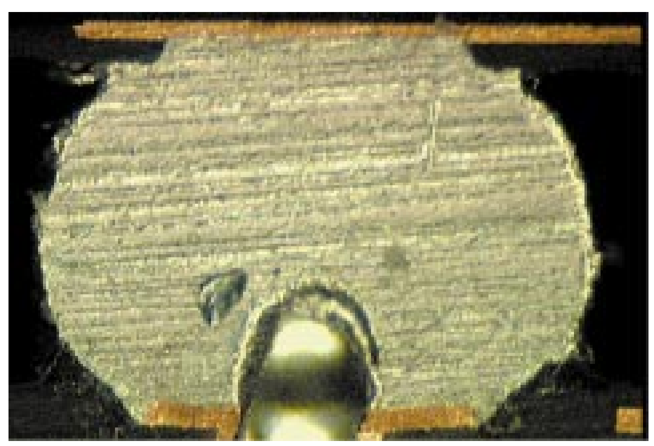


Figure 6-9 Cross Section of 0.75 mm Ball with Via-in-Pad Structure (Indent to the upper left of the ball is an artifact.)

When using via-in-pad technology, a void will occur in the joint as shown in Figure 6-11, unless the via is capped on

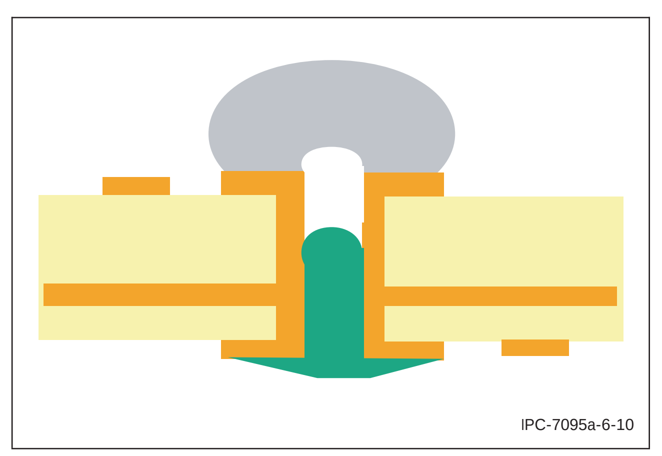


Figure 6-10 Cross Section of Via-in-Pad Design Showing Via Cap and Solder Ball

the component placement side of the board. Most experts agree that these void conditions, created due to entrapped air, are acceptable and have no impact on the reliability of the joint. There is no doubt that the conditions depend not only on the process, but the size of the BGA land and the diameter of the hole. In addition, there is a difference as to whether the hole is a through-hole, blind via, or microvia. Figure 6-11 shows the characteristics of the three hole configurations of what takes place at incoming, after the solder paste has been printed and the BGA has been placed; the conditions of the ball and hole during reflow soldering and finally, the characteristics of the resulting solder joint.

One of the major reasons for the occurrence of the void conditions is the entrapped gas that exists under the solder paste during the original paste printing and BGA place ment. During the reflow operation, the entrapped gas and the solder paste volatiles need to escape and this creates the minor occurrences of absence of solder at the center part of the ball as shown in the illustration.

6.4 Impact of Wave Solder on Top Side BGAs

6.4.1 Top Side Reflow Mixed Technology printed circuit boards are typically assembled by first reflow soldering the surface mount packages on the top side of the board and then wave soldering the through-hole packages (inserted from the top side) as well as the surface mount components on the bottom side. During the wave soldering process step, however, the reflow soldered surface mount components on the top side of the board are also heated. This heating can cause the solder joints of these components to melt if the temperature increases close to the liquidus point of the solder alloy. Hence, care needs to be taken to avoid

BGA

Incoming - Before Assembly Process

After Solder Paste Printing & BGA Placement

During Reflow Soldering

Post Reflow Soldering

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Figure 6-11 Via-In-Pad Process Descriptions

the solder joint of these components from reaching the liquidus temperature.

6.4.2 Impact of Top Side Reflow BGA solder joints need particular attention in this regard since the solder joints are under stress during the wave soldering operation. If these solder joints reach the liquidus temperature (183°C for the eutectic tin-lead composition) then there is a potential to de-wet or be pulled away from the board or the package substrate due to the thermo-mechanical strains induced in them at the elevated temperatures. Since solder is extremely soft even at temperatures approaching the liquidus temperature, the potential for cold solder, de-wetting or ball deformation exists when their temperatures do not reach liquidus.

Figure 6-12 depicts examples of ball deformation and de-wetting for a BGA component located on the top side of a motherboard. The solder joints of the BGA reached a peak temperature of 180°C during wave solder. BGAs are more prone to such defects than leaded surface mount solder joints since there is less strain relief.

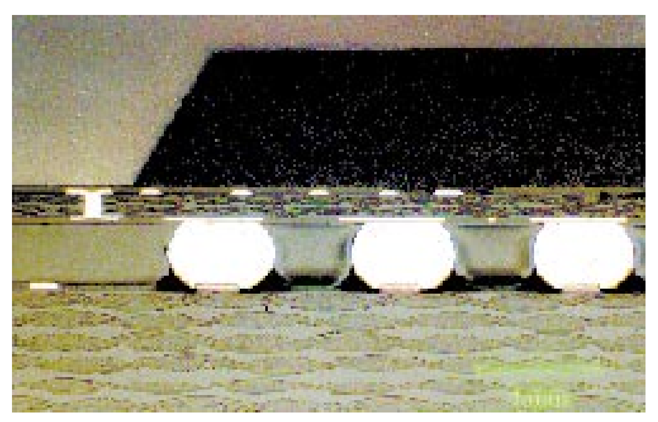


Figure 6-12 Example of Top Side Reflow Joints

To avoid problems in BGA solder joints on the top side of the board, their temperatures should not exceed 150°C during wave soldering. This is less than the maximum temperature allowed for the Fine Pitch Leaded components such as PQFPs.

Figure 6-13 is an example of an acceptable temperature profile for the solder joints on a mixed technology board during the wave solder process.

To determine the various ways of keeping the temperature below 150°C, it is best to first identify the various ways in which the BGA solder joints are heated during the wave solder process. Figure 6-14 illustrated three pathways. Pathway A is by conduction through the thickness of the board from bottom to top. Pathway B is by conduction through the barrel of the via, along a trace connecting the via to the BGA solder joint land. Pathway C is by convection and radiation from the Preheaters on the top in the wave solder machine.

6.4.3 Methods of Avoiding Top Side Reflow The methods of avoiding top side reflow aim to reduce the heat transfer to the BGA solder joints by one or more of the three pathways described above. Figure 6-15 illustrates these methods.

A heat shield can be placed over the BGA packages to avoid direct heating from the preheaters in the wave solder machine. These shields can be mechanically attached to the wave solder pallets.

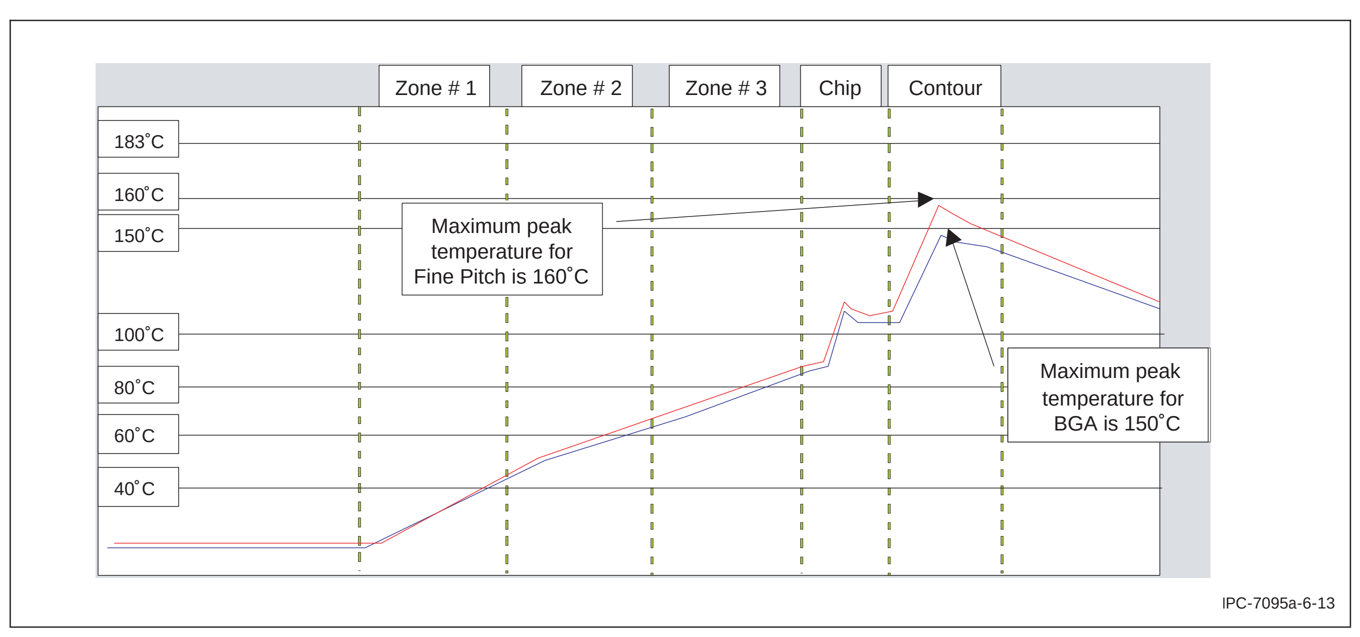


Figure 6-13 Example of Wave Solder Temperature Profile of Top-Side of Mixed Component Assembly

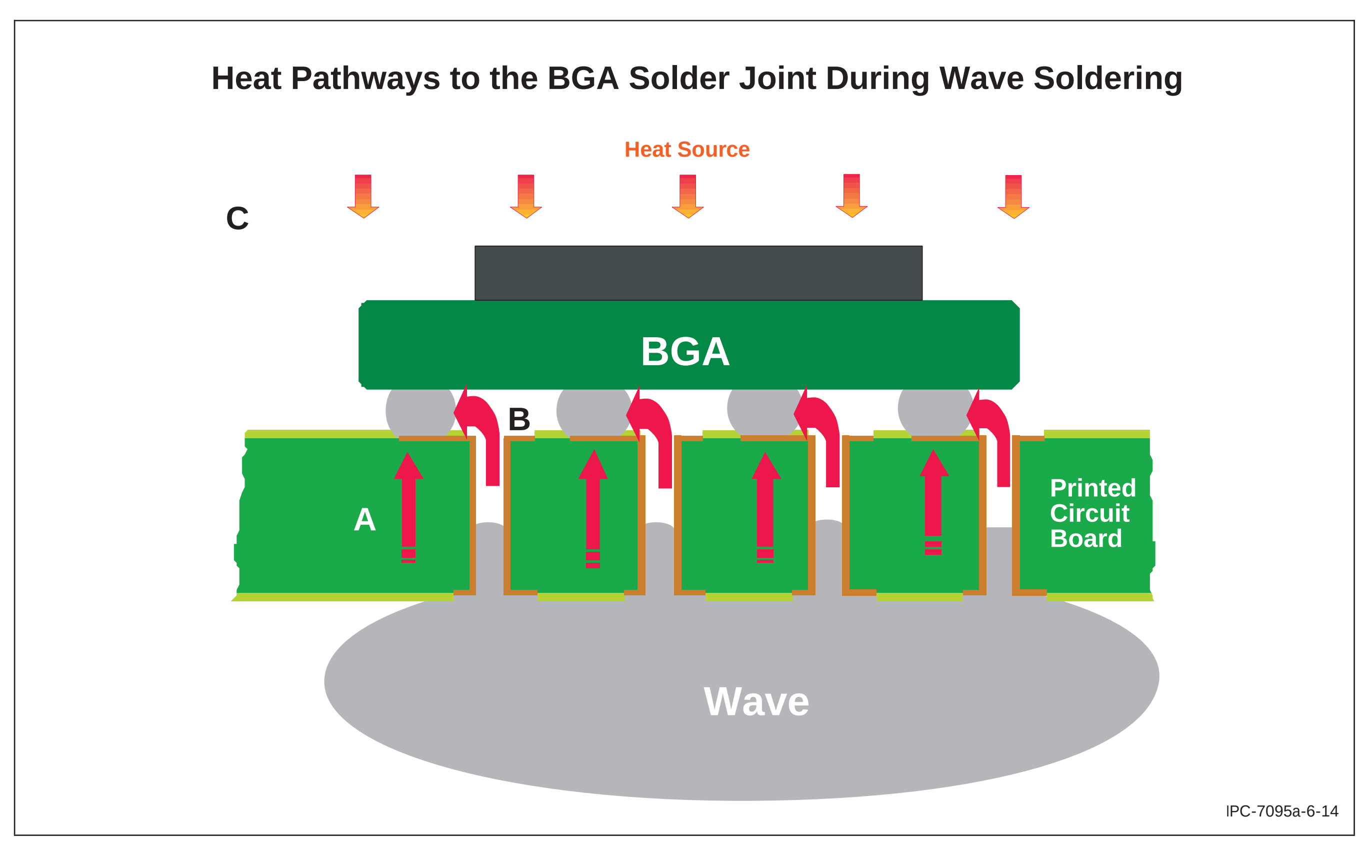


Figure 6-14 Heat Pathways to BGA Solder Joint During Wave Soldering

Methods of Avoiding Topside BGA Solder Joint Reflow During Wave Soldering

Heat Source

Heat Shield (Attached to Pallet)

BGA

Printed Circuit Board

Nonmetallic Wave Shield (Attached to Pallet)

Via Capping

Wave

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Figure 6-15 Methods of Avoiding BGA Topside Solder Joint Reflow

Secondly, vias can be capped by solder mask on the bottom side of the board. This via-capping process is very commonly employed in the industry, for a variety of reasons. Via capping rules should be built into the Design for Manufacturability (DFM) process, during board design.

Vias that certainly need to be capped are those that are connected to the BGA land with a short trace length or those that are connected to a plane in the board.

Thirdly, a nonmetallic wave shield can be placed immediately below the BGA package locations on the bottom side of the board to avoid the wave from touching these board locations. The wave shield can also be attached to the wave pallet by nonmetallic fingers.

The efficacy of each of these methods should be confirmed by measuring the temperature profile of the BGA solder joints during the wave solder process and ensuring that they stay below 150°C.

6.4.4 Top Side Reflow for Lead Free Boards Most lead free solders targeted for use, including the popular solders in the SnAgCu system, have melting points higher than that for eutectic SnPb solder. Hence, the potential for top side reflow when wave soldering boards with surface mount lead free components already reflow soldered on the top side of the board is significantly reduced. For SnAgCu solders, the maximum top side solder joint reflow temperature can reach 190°C without any impact on the BGA solder joints.

6.5 Testability and Test Point Access The differences in contact design have differing effects on the quality and reliability of the contact, contactability, and later solderability. The effects are negligible and insignificant when the contact is minimal.

6.5.1 Component Testing As the BGA pitches and solder ball size decrease, socket manufacturers face increasing challenges in the design of sockets to adequately test BGA packages. There are a myriad of tip designs socket manufacturers are working with to meet the needs of sub-mm pitch BGAs.

One challenge is to be able to make contact to all BGA individuals balls. While attaching to a PCB, the solder balls melt and self align to attach to the corresponding lands on the PCB. Therefore, wider variations in the placements of solder balls are tolerable with respect to BGA attach to the PCB. But these variations need to be tightened in the case of test and burn-in and thus there is no self-alignment of solder balls to socket contacts.

The design of socket probes need to take into account the solder ball height variation. A larger variation in solder ball height would require a wider reach range for socket probes, and also when testing, the solder balls will be more vulnerable. Burn-in of BGAs is conducted at an elevated temperature. The burn-in time/temperature combination will soften the solder balls to an extent dependent upon the solder ball material. Under test probe pressure, the softened solder ball will deform heavily and may affect the contact quality during burn-in. The socket manufacturers need to assure that the probes do not stick to softened solder balls and the solder balls are not pulled away.

The socket test probe design is also critical in that the probe does not gouge the solder ball in such a way or to such an extent that the deformation becomes a quality or reliability concern during or after BGA attach to the PCB. Some contacts touch the solder ball on their sides, and some on the tip of the solder balls. In some designs, the individual pins are spring-loaded, in others all contact probes are in the same rigid plane.

6.5.2 Damage to the Solder Balls During Test and Burn-In In their pristine form, solder balls on a BGA are shiny and quite round. Their attach, handling and subsequent BGA processing steps may induce deformation, damage, pokes and dents.

The solder ball deformation during test and burn-in is an expected phenomenon and as such is an acceptable anomaly as long as it does not affect the usefulness of the product. Many contact designs exist, each vying for a better share of the market. Each contact will impart its unique imprint on the solder ball. These probes contact the solder ball at differing locations and impart unique imprints characteristic of the contact design to the solder ball during test and burn-in.

Solder balls have been known to come off in certain situations. Rather than trying to catch the problem by using vision systems to detect the presence or absence of solder balls or the damage to solder balls during testing, it is prudent to optimize the solder attachment and to choose a test socket which is benign to the device under test.

Some contacts disturb only the sides of the solder ball and not the bottom. The bottom of the solder ball is untouched during contact. One such example is shown in Figure 6-16.

Other contacts impact the bottom of the solder ball. Figure 6-17 shows a solder ball which has been contacted at the bottom of the solder ball. The concern is that, during reflow, flux may get entrapped in the depressions formed by the contact and may explode under reflow heat, splattering solder around, causing shorts, etc.

Some contacts are designed not to allow the entrapment of flux. Contact-probes may contact the bottom of solder ball to create a pattern which provides a path for the flux to escape and will not entrap flux during reflow.

Other contact impressions allow the entrapment of flux. If the impressions cause a hole at the bottom of the solder

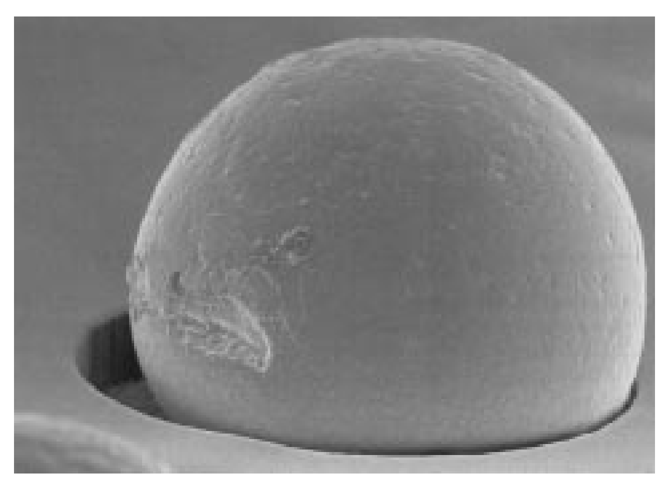


Figure 6-16 An Example of a Side Contact Made With a Tweezers Type Contact

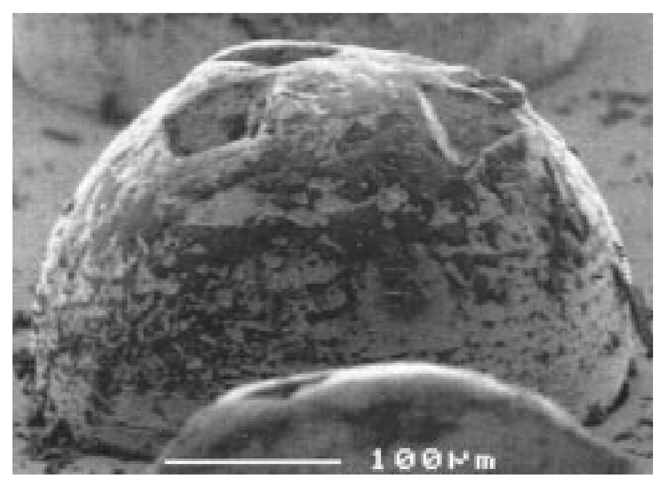


Figure 6-17 Pogo-Pin Type Electrical Contact Impressions on the Bottom of a Solder Ball

ball then there is a greater chance of flux entrapment. Such entrapment may be quite benign for shallow depressions. To be damaging, the depressions have to be larger than anticipated with current designs to entrap enough flux to cause problems.

Some contacts are designed with individual force mechanisms for each contact pin. Other contacts come with common force mechanism applied to all contacts simultaneously. All different kinds of contacting mechanisms will leave some imprint on the solder balls. Contact size should be matched with the solder ball size to be tested to minimize the solder ball deformation. Therefore, the size of the contact needs to decrease with decreasing solder ball sizes and decreasing array pitches. Too large of a contact size may short and may subject the solder ball to undesired levels of deformation.

The force mechanism to assure contact needs to match the solder ball hardness, which is dependent upon the solder constituents. Too much force will impart unnecessary deformation. The force mechanism needs to provide enough force to contact the smallest balls in an array. The solder balls soften when subjected or exposed to elevated temperatures and time durations. Force mechanism design needs to take this change in consideration for their use at varying temperatures. Even at ambient, continuous testing of parts may increase the temperature at the contact site.

For all practical purposes, the solder ball needs to be solderable with acceptable contact strength, contact area and solder column shape after it has endured the rigors of testing and burn-in. To assess the impact of processing through test and burn-in, the items to look at should include solderability, coplanarity, and general cosmetic shape of the solder ball. The solder ball should not lose so much solder to the test and burn-in process that enough solder is not left for optimum connection. The ball should be able to respond to the reflow process to produce an acceptable contact. Ball corrosion and foreign material pick up during test and burn-in should not adversely affect the quality and long-term reliability of the solder ball. After the test and burn-in cycle, especially for no-melt balls, meeting the coplanarity expectations will be an essential requirement for proper BGA attachment to substrate.

Various contact technologies contact differing parts of the solder ball. In fact most of the contact designs touch the bottom of the solder ball to make a contact. In view of these options, it would be impossible to declare certain parts of the solder ball untouchable during its processing. To keep a certain area of the solder ball untouchable is neither practical nor necessary if it has no effect on solderability, coplanarity, solder volume, quality and reliability of the end product.

6.5.3 Bare Board Testing There are a number of issues that arise when considering the test inspection and measurement of increasingly complex substrate interconnections especially when involved with the electrical evaluation of the substrate. In order for the manufacturer to be able to reduce cost while adequately assuring the electrical function of the substrate interconnection, the customer will have to provide definitive test data, with the preference being 100% netlist testing. Compatibility of the data is currently an issue as well. It is hoped that industry standardization efforts will help to solve this issue in the foreseeable future. One item which could prove key to achieving this is likely to be acceptance of a standard base grid pitch, which would allow test equipment and socket manufacturers to examine and focus on creation of a universal solution.

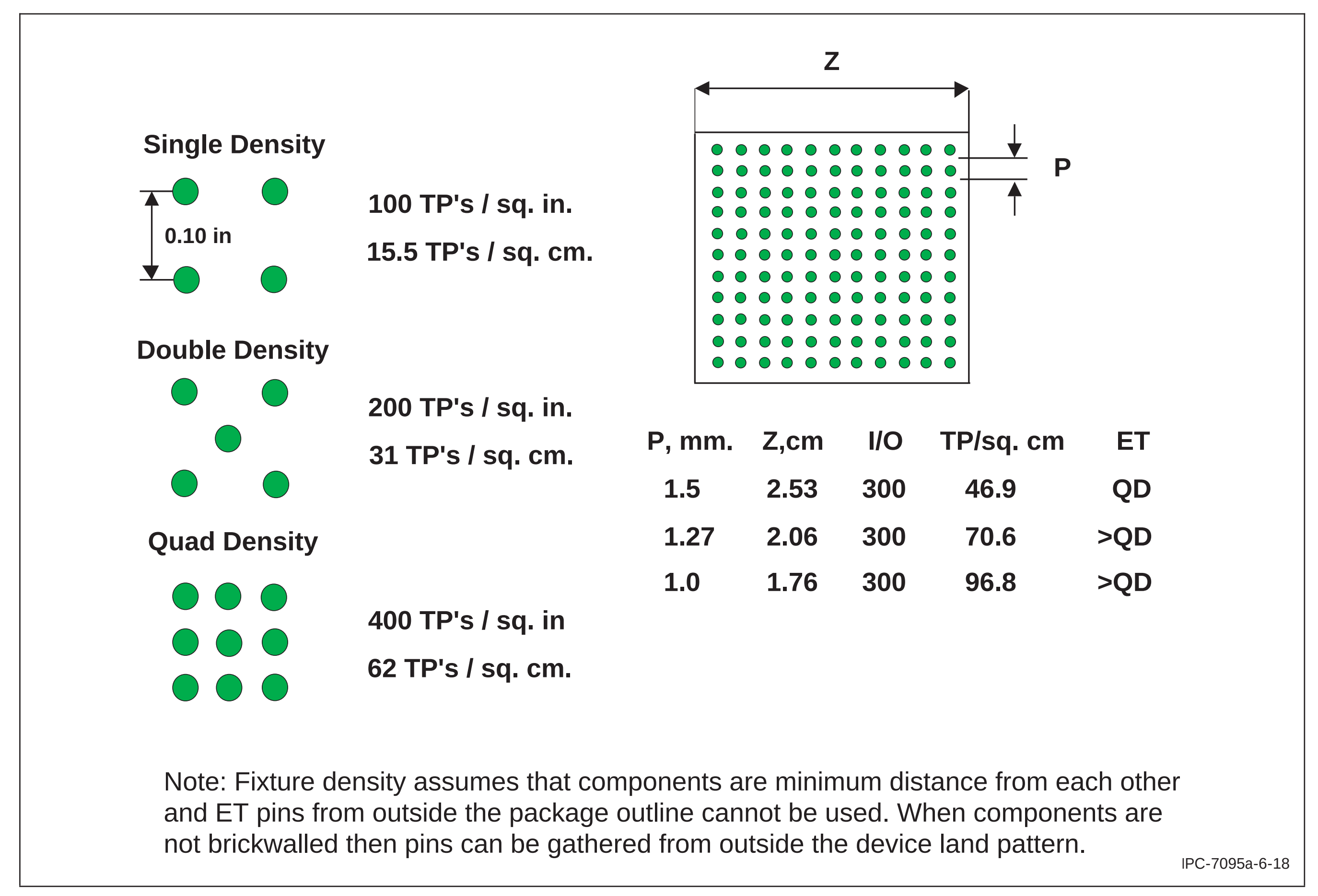
The use of fixtures and bed of nails testing for opens and shorts testing is quickly losing the ability to meet test requirements as feature size decreases, coupled with increased densities. Double density, or 1.77 mm pitch, test beds seem to be adequate for 400 µm pitch and up. As the density of the substrate increases beyond 400 µm pitch, alternative techniques must be considered. Quad density

fixturing is a possibility, with 62 test probes per square centimeter, but concern increases about potential feature damage due to the contact by the probes. In addition, the cost of double and quad density fixtures, as well as the cost of test equipment, make it difficult to justify total test coverage within cost expectations based on current understanding of electrical testing and a linear projection of present testing concepts.

Regarding the I/O density of 200 to 1000 at various grid segmentation, it becomes apparent that double and quad density is capable for bare board continuity testing the average I/O requirements. However, if components are stacked ''edge-to-edge'' the testing becomes impossible with this test approach. This is because a BGA on 1.0 mm pitch contains 96 lands per cm^2, and the quad density test fixture is only able to accommodate 62 probes per cm^2. Spreading components on the mounting structure relieves some of that complexity but also consumes more space and reduces performance. It should also be noted that, using presently available testing concepts, maximum component I/O creates a condition that drives testing cost of the bare board dramatically higher due to multi-pass or dual fixture testing in order to have full test coverage. Figure 6-18 shows the relationship of part land requirements compared to fixture capability.

Flying probe testing eliminates the need for costly fixtures and, depending on the volume of substrates being manufac tured, can provide a cost-effective alternative to bed of nailstesting. Unfortunately, the test is relatively slow, depending on the equipment used, and the equipment can be expensive. The problem is compounded by the increased density requirements and the need for additional net testing. Most of this equipment/test technique has evolved from the semiconductor industry and has experienced some difficulty in scaling to meet the mechanical challenges associated with larger panel sizes. In addition, the small feature size in some instances defeat the detection system due to the difficulties in charging the feature with the probe. Additional equipment development will have to take place if technologies such as this are going to be useful for the complex substrates of the future.

As via size continues to decrease, the limits of conventional evaluation with metallographic microsection will become less viable. 150 µm vias seem to be the practical limit for microsection labs of average competence. An alternative test method will be required if companies want to know more about the plating in the via than just continuity. An electrical Interconnect Stress Test is presently being used by some companies to determining hole integrity and reliability.



P, mm.	Z,cm	I/O	TP/sq. cm	ET
1.5	2.53	300	46.9	QD
1.27	2.06	300	70.6	>QD
1.0	1.76	300	96.8	>QD

Figure 6-18 Area Array Land Pattern Testing

6.5.4 Assembly Testing Design of a printed board assembly for testability normally involves systems level testability issues. In most applications, there are system level fault isolation and recovery requirements such as mean time to repair, percent up time, operate through single faults, and maximum time to repair. To meet the contractual requirements, the system design may include testability features, and many times these same features can be used to increase testability at the printed board assembly level. The printed board assembly testability philosophy also needs to be compatible with the overall integrations, testing and maintenance plans for the contract. The factory testers to be used, how integration and test is planned, when printed board assemblies are conformal coated, the depot and field test equipment capabilities and personnel skill level are all factors that must be considered when developing the printed board assembly test strategy.

The test philosophy may be different for different phases of the program. For example, the first unit debug philosophy may be much different than the test philosophy for spares when all the systems have already been shipped. Before the PWB design starts, requirements for the system testability functions should be presented at the conceptual design review. These requirements and any derived requirements should be partitioned down to the various printed board assemblies and documented. The system and program level test criteria and how they are partitioned down to the printed board assembly requirements are beyond the scope of this document.

The two basic types of printed board assembly test are functional test and in-circuit test. Functional testing is used to test the electrical design functionality. Functional testers access the board under test through the connector, test points, or bed-of-nails. The board is functionally tested by applying predetermined stimuli (vectors) at the printed board assembly's inputs while monitoring the printed board assembly outputs to ensure that the design responds properly.

In-circuit testing is used to find manufacturing defects in printed board assemblies. In-circuit testers access the board under test through the use of a bed-of-nails fixture which makes contact with each node on the printed board assembly. The printed board assembly is tested by exercising all the parts on the board individually. In-circuit testing places less restrictions on the design. Conformal coated printed board assemblies and many Surface Mount Technology (SMT) and mixed technology printed board assemblies present bed-of-nails physical access problems which may prohibit the use of in-circuit testing. Primary concerns for in-circuit test are that the lands or pins (1) must be on grid (for compatibility with the use of bed-of-nails fixture) and (2) should be accessible from the bottom side (a.k.a. non-component or solder side of through-hole technology boards) of the printed board assembly.

Manufacturing Defects Analyzer (MDA) provide a low cost alternative to the traditional in-circuit tester. Like the in-circuit tester, the MDA examines the construction of the printed board assembly for defects. It performs a subset of the types of tests, mainly only tests for shorts and opens faults without power applied to the printed board assembly. For high volume production with highly controlled manufacturing processes (i.e., Statistical Process Control techniques), the MDA may have application as a viable part of a printed board assembly test strategy.

Vectorless Test is another low cost alternative to in-circuit testing. Vectorless Test performs testing for finding manufacturing process-related pin faults for SMT boards and does not require programming of test vectors. It is a powered-off measurement technique consisting of three basic types of tests:

1. ***Analog Junction Test –*** DC current measurement test on unique pin pairs of the printed board assembly using the ESD protection diodes present on most digital and mixed signal device pins.
2. ***RF Induction Test –*** Magnetic induction is used to test for device faults utilizing the printed board assemblies devices protection diodes. This technique uses chip's power and ground pins to make measurements for finding solder opens on device signal paths, broken bond wires, and devices damaged by ESD. Parts incorrectly oriented can also be detected. Fixturing containing magnetic inducers are required for this type of test.
3. ***Capacitive Coupling Test –*** This technique uses capacitive coupling to test for pin opens and does not rely on internal device circuitry but instead relies on the presence of the metallic lead frame of the device to test the pins. Connectors and sockets, lead frames and correct polarity of capacitors can be tested using the technique.

6.5.4.1 Functional Testing Concerns There are several concerns for designing the printed board assembly for functional testability. The use of test connectors, problems with initialization and synchronization, long counter chains, self diagnostics, and physical testing are topics which are discussed in detail in the following subsections and are not meant to be tutorials on testability but rather ideas of how to overcome typical functional testing problems. Fault isolation on conformal coated boards or most SMT and mixed technology designs can be very difficult because of the lack of access to the circuitry on the board. If strategic signals are brought out to a test connector or an area on the printed board where the signals can be probed (test points), fault isolation may be much improved. This lowers the cost of detection, isolation and correction. It is also possible to design the circuit so that a test connector can be used to stimulate the circuit (such as taking over a data bus via the test connector) or disable functions on the printed board assembly (such as disabling a free running

oscillator and adding single step capability via the test connector).

6.5.4.2 In-Circuit Test Concerns In-circuit testing is used to find shorts, opens, wrong parts, reversed parts, bad devices, incorrect assembly of printed board assemblies and other manufacturing defects. In-circuit testing is neither meant to find marginal parts nor to verify critical timing parameters or other electrical design functions.

In-circuit testing of digital printed board assemblies can involve a process that is known as backdriving (see IPC-T-50). Backdriving can also cause devices to oscillate and the tester can have insufficient drive to bring a device out of saturation. Backdriving can be performed only for controlled periods of time, or the junction of the device (with the overdriven output) will overheat.

The two main concerns for designing the printed board and printed board assembly for in-circuit testability are design for compatibility with in-circuit test fixturing and electrical design considerations.

6.6 Other Design for Manufacturability Issues The layout generation process should include a formal design review of layout details by as many affected disciplines within the company as possible, including fabrication, assembly and testing. The approval of the layout by representatives of the affected disciplines will ensure that these production-related factors have been considered in the design. The success or failure of an interconnecting structure design depends on many interrelated considerations. From an end-product usage standpoint, the impact on the design by the following typical parameters should be considered. Other design for manufacturability issues include:

- Equipment environmental conditions, such as ambient temperature, heat generated by the components, ventilation, shock and vibration.
- If an assembly is to be maintainable and repairable, consideration must be given to component/circuit density, the selection of board/conformal coating materials, and component placement for accessibility.
- Installation interface that may affect the size and location of mounting holes, connector locations, lead protrusion limitations, part placement, and the placement of brackets and other hardware.
- Testing/fault location requirements that might affect component placement, conductor routing, connector contact assignments, etc.
- Process allowances such as etch factor compensation for conductor widths, spacings, land fabrication, etc.
- Manufacturing limitations such as minimum etched features, minimum plating thickness, board shape and size, etc.
- Coating and marking requirements.
- Assembly technology used, such as surface mount.
- Through hole, and mixed.
- Board performance class.
- Materials selection.
- Producibility of the printed board assembly as it pertains to manufacturing equipment limitations.
  – Flexibility (Flexural) Requirements.
  – Electrical/Electronic.
  – Performance Requirements.
- ESD sensitivity considerations.

6.6.1 Panel/Subpanel Design Panelization of parts is a standard process for both test and assembly. A datum system is required for the panel, as well as each individual board in the panel. To reduce tolerance buildup, it is important to relate each individual board datum to the panel datum (see Figure 6-19).

Most assembly companies want to build the assembly in array format, similar to that shown in Figure 6-19. The board manufacturer of these subpanels would position the subpanels on the standard manufacturing panel, which is usually 460 x 610 mm. Designers are encouraged to work with their manufacturing suppliers in order to optimize the material movement, and the manner in which the panels/boards are removed from their respective position and how they are tested.

6.6.2 In-Process/End Product Test Coupons Coupons have been used by the industry for many years in an effort to evaluate the product being built. These coupons represented the features of the board or the features of the assembly. They are incorporated into the borders of the panels either used for board manufacturing or the subpanels provided to the assembly company. Known as quality conformance coupons, they were many times evaluated once the product had been completely manufactured. This technique is no longer valid in that the concepts of inspecting the quality into the product have not borne fruit. Most manufacturers and assemblers have their processes in control, nevertheless, coupons are of value to make certain through various physical evaluations that the process and the recipe used to make the part stay in the control that is necessary to meet requirements. This concept is essential for BGAs since one cannot see the lands or the solder joints once the assembly has taken place. Test coupons or specimens should reflect the specific board or panel characteristics. The data derived from panels should be used to establish the requirements for vias and lands, conductors, spaces, etc. When specimens are used to establish process control parameters, they shall consistently use single hole size or land configuration which reflects the process. Process characteristics and general board characteristics should be matched.

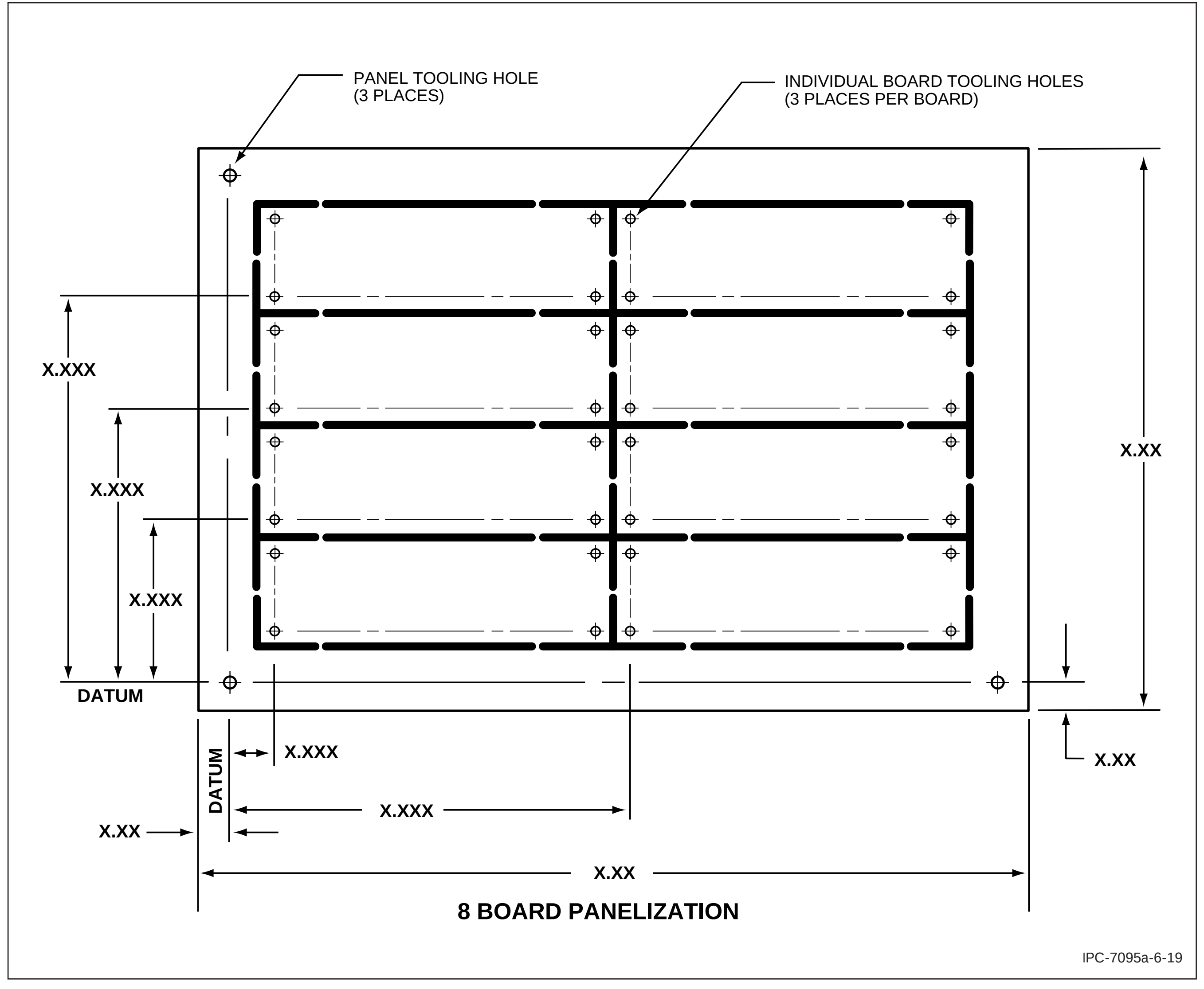


Figure 6-19 Board Panelization

IPC-2221 provides excellent coupons that are used to evaluate those board and assembly characterizations. They include:

- Hole Solderability
- Solder Resist Tenting
- Thermal Stress Plating
- Thickness and Bond Strength
- Plating Adhesion
- Surface Solderability
- Solder Resist
- Surface Mount Solderability
- Surface Bond Strength
- Surface Insulation Resistance
- Moisture Insulation Resistance
- Registration
- Interconnect Resistance

Figure 6-20 shows an alternate coupon that can be used to evaluate the cleanliness of a board after ball attachment has been completed. This comb pattern is used on the board in order to make certain that flux or flux residue does not impair the electrical properties of the product.

6.7 Thermal Management The primary objective of thermal management is to ensure that all circuit components, especially the BGAs, are maintained within both functional and maximum allowable limits. The functional temperature limits provide the ambient or component package (case) temperature range within which the electronic circuits can be allowed to properly perform.

The cooling technique to be used in the printed board assembly applications must be known in order to ensure the proper printed board assembly design. For commercial applications, direct-air cooling (i.e., where cooling air contacts the printed board assembly), is usually used.

For rugged and hostile usage, indirect cooling must be used to cool the printed board assembly. In this application, the

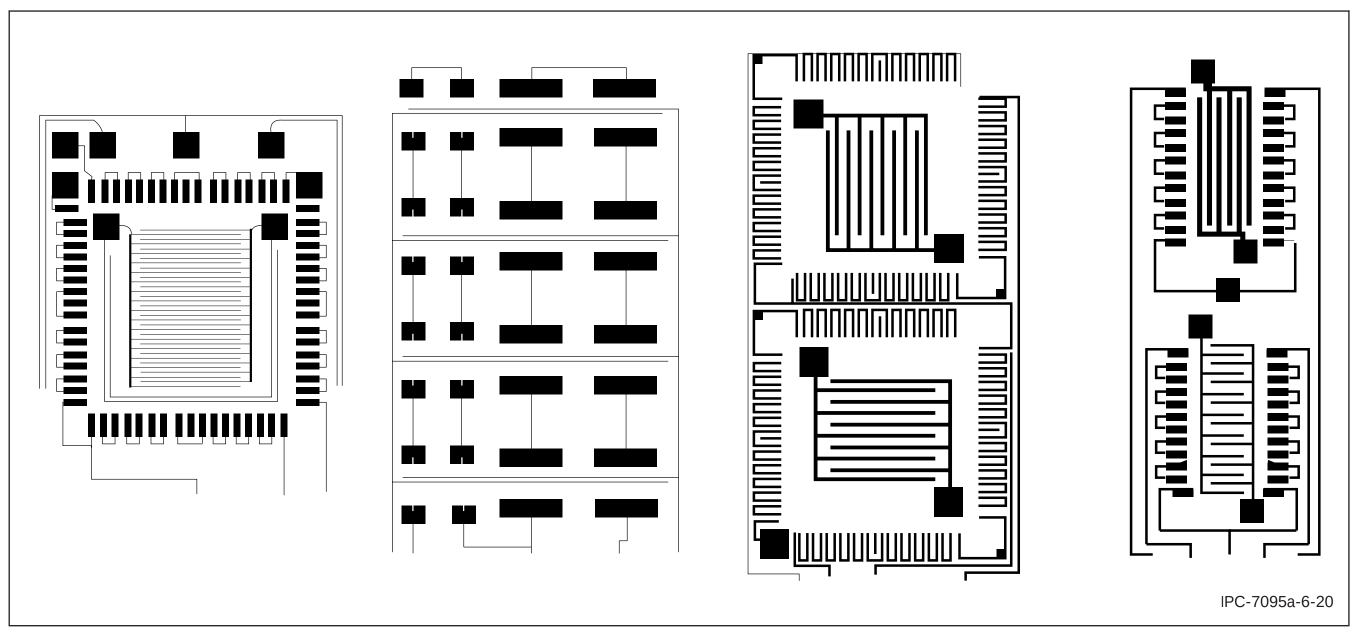


Figure 6-20 Comb Pattern Examples

assembly is mounted to the structure that is air or liquid cooled and the components are cooled by the conduction through a heat exchange surface. These designs must use appropriate metal heatsinks on the printed board assembly. Appropriate component mounting and bonding may be required. To ensure adequate design, thermal dissipation maps must be provided to aid analysis and thermal design of the printed board assembly.

The dissipation of heat generated within electronic equipment results from the interaction of the three basic modes of heat transfer: conduction, radiation, and convection. These heat transfer modes can, and often do, act simultaneously. Thus, any thermal management approach should attempt to maximize their natural interaction.

6.7.1 Conduction The first mode of heat transfer to be encountered is conduction. Conduction takes place to a varying degree through all materials. The conduction of heat through a material is directly proportional to the thermal conductivity constant (K) of the material, the cross sectional area of the conductive path and the temperature difference across the material. Conduction is inversely proportional to the length of the path and the thickness of the material (see Table 6-3).

6.7.2 Radiation Thermal radiation is the transfer of heat by electromagnetic radiation, primarily in the infrared (IR) wavelengths. It is the only means of heat transfer between bodies that are separated by a vacuum, as in space environments.

Heat transfer by radiation is a function of the surface of the ‘‘hot’’ body with respect to its emissivity, its effective surface area and the differential to the fourth power of the absolute temperatures involved.

The emissivity is a derating factor for surfaces that are not ‘‘black bodies.’’ It is defined as the ratio of emissive power of a given body to that of a black body, for which emissivity is unity (1.0). The optical color of a body has little to do with it being a ‘‘thermal black body.’’ The emissivity of anodized aluminum is the same if it is black, red or blue. However, surface finish is important. A matte or dull surface will be more radiant than a bright or glossy surface (see Table 6-4).

Devices, components, etc. close to one another will absorb each others’ radiant energy. If radiation is to be the principle means of heat transfer, ‘‘hot’’ spots must be kept clear of each other.

6.7.3 Convection The convection heat transfer mode is the most complex. It involves the transfer of heat by the mixing of fluids, usually air.

The rate of heat flow by convection from a body to a fluid is a function of the surface area of the body, the temperature differential, the velocity of the fluid and certain properties of the fluid.

The contact of any fluid with a hotter surface reduces the density of the fluid and causes it to rise. The circulation resulting from this phenomenon is known as ‘‘free’’ or ‘‘natural’’ convection. The air flow can be induced in this manner or by some external artificial device, such as a fan or blower. Heat transfer by forced convection can be as much as ten times more effective than natural convection.

6.7.4 Thermal Interface Materials Attachment of heat sinks to BGAs is the most common technique today in cooling the silicon devices packaged within the BGAs. These heat sinks require a thermal interface material to be

Table 6-3 Effects of Material Type on Conduction Materials

Materials	Thermal Conductivity (K)		
	Watts/inch °C	Watts/m °C	Gram-calorie/cm °C • s
Still Air	0.0007	0.0276	0.000066
Epoxy	0.005	0.200	0.00047
Thermally Conductive Epoxy	0.02	0.787	0.0019
Aluminum Alloy 1100	5.63	222	0.530
Aluminum Alloy 3003	4.88	192	0.459
Aluminum Alloy 5052	3.52	139	0.331
Aluminum Alloy 6061	4.36	172	0.410
Aluminum Alloy 6063	4.88	192	0.459
Copper	4.93	194	0.464
Steel Low Carbon	1.19	46.9	0.112

Table 6-4 Emissivity Ratings for Certain Materials

Material and Finish	Emissivity
Aluminum Sheet - Polished	0.040
Aluminum Sheet - Rough	0.055
Anodized Aluminum - any color	0.80
Brass - Commercial	0.040
Copper - Commercial	0.030
Copper - Machined	0.072
Steel - Rolled Sheet	0.55
Steel - Oxided	0.667
Nickel Plate - Dull Finish	0.11
Silver	0.022
Tin	0.043
Oil Paints - Any Color	0.92-0.96
Lacquer - Any Color	0.80-0.95

sandwiched between the heat sink and the BGA in order to conduct the heat from the top of the package surface and into the bottom of the heat sink surface.

When selecting a thermal interface material, keep in mind the surface flatness of the BGA body and the heatsink. Warpage of the BGA package during reflow and large tolerances on the heatsink contact surface can result in large gaps that are difficult to fill reliably with some interface materials. This in turn can cause poor thermal conductivity and/or a weak heatsink attachment bond.

There are various types of thermal interface materials (TIM). These are described below.

Adhesives: Metal filled epoxies and silicone adhesives were commonly used as TIMs initially. They play a dual part of being a TIM as well as a mechanical attachment method since when cured they become highly cross-linked and attain high cohesive strength. Hence, unlike the other TIMs, supplementary mechanical attachment methods are not necessary when using adhesive. Disadvantages of adhesives include a thermal cure step being necessary after the BGA is soldered on the board and the potential for severe delamination at the interfaces that the adhesive bonds to due to coefficient of thermal expansion mismatches between the heat sink and the package. Another subclass of adhesives are the pressure sensitive adhesives (PSA), which do not require a cure to generate the interfacial bond, but instead require a certain amount of pressure, typically in the 20 to 30 psi range. Their use for BGAs is therefore limited since this pressure, if not properly controlled, may adversely impact the BGA solder joints.

Greases: Thermal greases are metal filled polymers that have the inherent advantage of being 'liquidy' and conforming to the macroscopic and microscopic irregularities in the surfaces of the heat sink and the BGA component. They have excellent thermal performance and unlike adhesives do not require a cure. Two major disadvantages of thermal greases are that they tend to migrate out from between the heat sink and package interfaces over time. This phenomenon is known as 'pump out' and is caused by the thermo-mechanical stresses exerted at the interfaces during temperature cycling.

Phase Change Materials (PCM): Phase change materials are in a solid state at room temperature but become liquid at the higher temperatures at which they are required to conduct heat away from the BGA surface. Hence, they offer ease of handling and dispensing because they typically are in a film form and do not need to be cured. However, their thermal conduction properties are inferior to greases, adhesives and the other TIM alternatives and hence they are suitable for use with only low wattage devices.

Gels: Gels are comprised of a lightly cross-linked silicone polymer filled with metal or ceramic particles that impart the thermal conductivity necessary for this TIM. Gels combine the beneficial properties of greases and cured adhesives, do not pump-out and do not require post application cure step. Their modulus is low enough to relieve thermo-mechanical stresses and avoid interfacial delaminations. They have high bulk thermal conductivities are have seen use in cooling BGA components containing high wattage CPU devices.

6.7.5 Heat Sink Attachment Methods for BGAs There are quite a few techniques for attaching heat sinks to BGAs. These are depicted in the following illustrations.

Figure 6-21 shows a heat sink attached to the top of a BGA package with a thermally conductive adhesive. The adhesive acts as both a thermal conduction medium as well as a mechanical attachment medium. As mentioned above, however, this technique requires a post solder thermal cure step to cross-link the adhesive and harden it.

Figure 6-22 illustrates a heat sink attached to the top of a BGA package with clips that hook on to a BGA substrate. The thermal interface material in this case is a grease, or PCM or gel, i.e., one that does not provide a strong mechanical bond between the heat sink and the top of the BGA package. This method has one drawback. The weight of the heat sink is supported by the package and during mechanical shock and vibration the solder balls of the BGA have to bear the mechanical stresses generated by the additional mass of the heat sink.

Figure 6-23 depicts the case of a heat sink attached to the BGA with clips that hook into holes in the printed circuit board. These holes do not have to be plated. Unlike the previous case, the printed circuit board supports the weight of the heat sink when the clips are actuated, but some stress can still be transferred on to the BGA solder balls during mechanical shock and vibration.

Figure 6-24 shows the case of a heat sink attached to a BGA package with clips that hook on stakes that are wave soldered into holes in the printed circuit board. This method of attachment transfers even less stress on the BGA

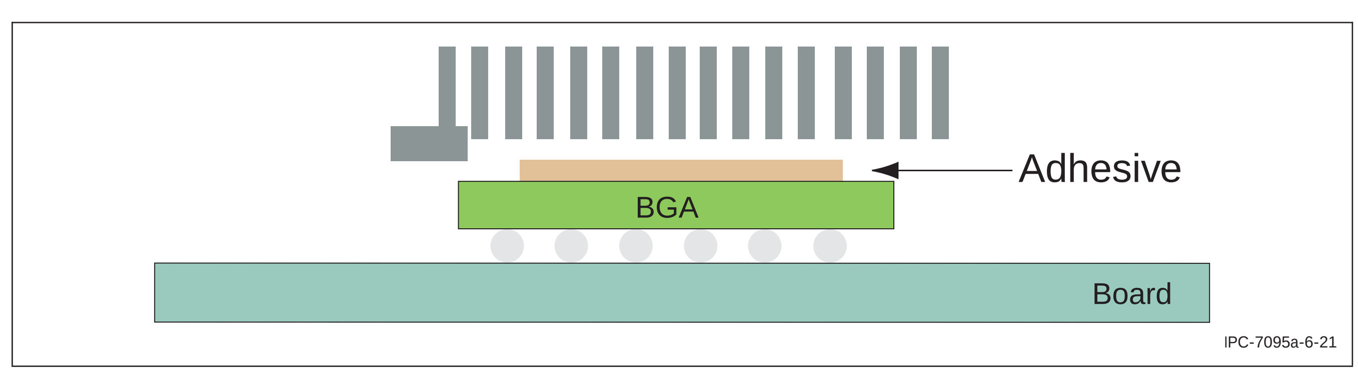


Figure 6-21 Heat Sink Attached to a BGA with an Adhesive

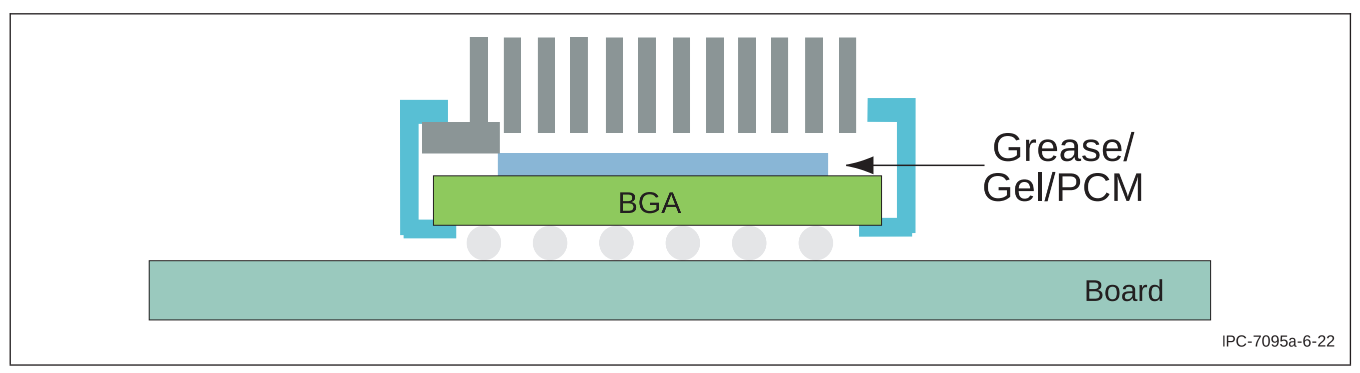


Figure 6-22 Heat Sink Attached to a BGA with a Clip that Hooks onto the Component Substrate

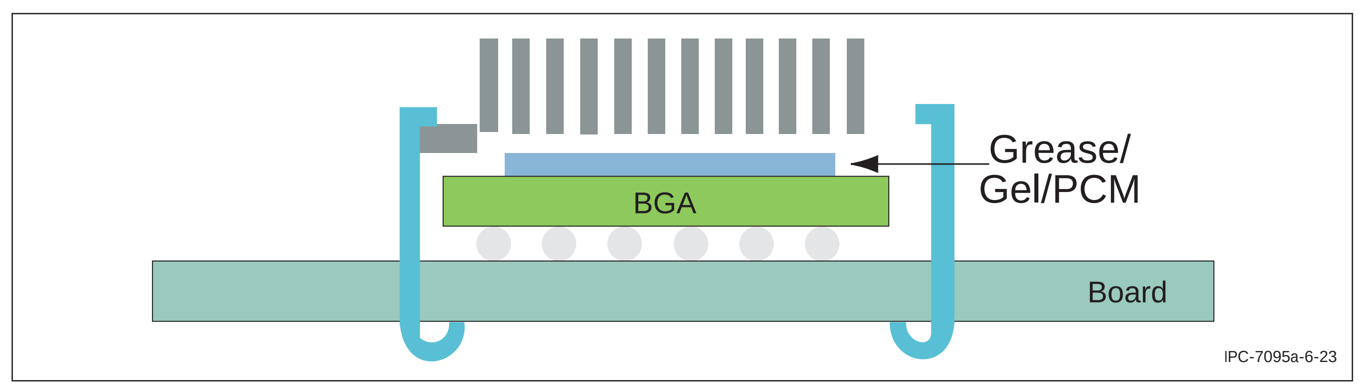


Figure 6-23 Heat Sink Attached to a BGA with a Clip that Hooks into a Through-Hole on the Printed Circuit Board

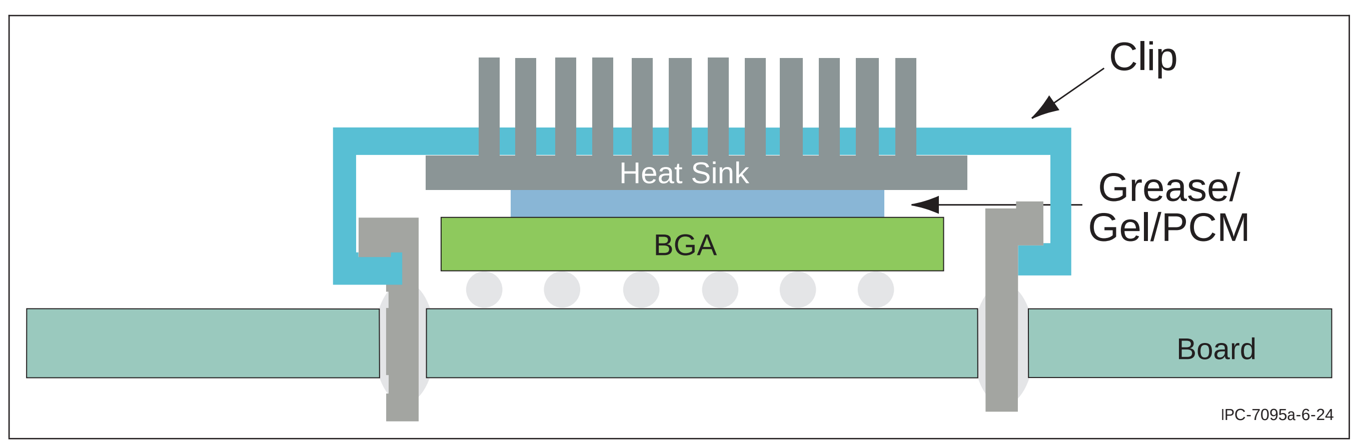


Figure 6-24 Heat Sink Attached to a BGA with a Clip that Hooks onto a Stake Soldered in the Printed Circuit Board

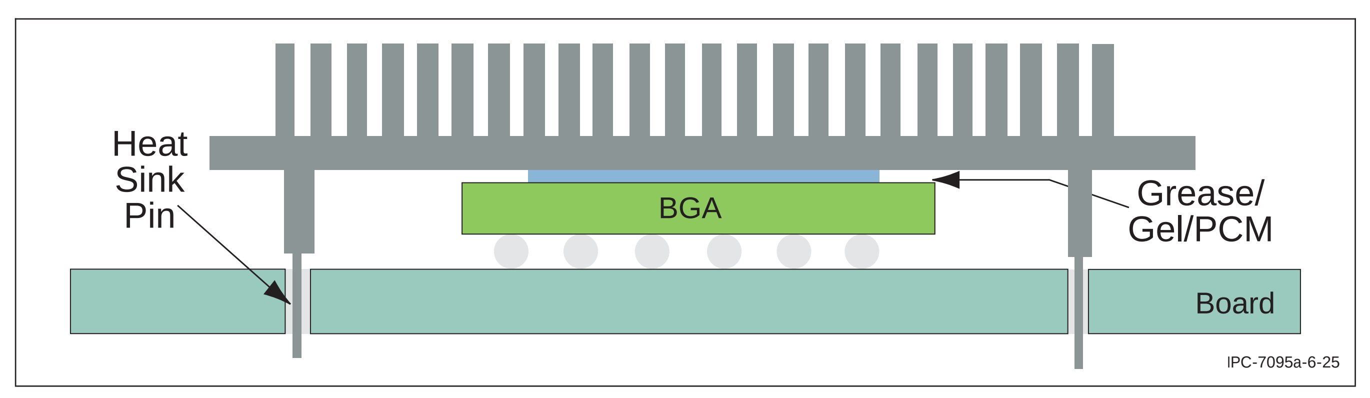


Figure 6-25 Heat Sink Attached to a BGA by Wave Soldering its Pins in a Through-Hole in the Printed Circuit Board

solder balls than the previous case during mechanical shock and vibration. However, the solder joints of the stakes will bear most of this stress.

Figure 6-25 illustrates the attachment of the heat sink to a BGA by directly soldering the heat sink into the board during the wave soldering process step. The heat sink design has four or more pins that insert into holes in the board prior to the wave solder process. As opposed to the previous cases above, this method does not need any post assembly processing to attach the heat sink.

The three methods in Figures 6-23, 6-24 and 6-25 have one drawback not present in the first two. These methods require holes in the printed circuit to be designed in. These holes may reduce the trace routing real estate on all the board layers. For highly dense board designs, this could impact the final layer count of the board.

6.8 Documentation The documentation package for describing BGA components usually consists of a master drawing, master pattern drawing, copies of artwork (film or paper), mounting structure assembly drawing, parts list, and schematic/logic diagram. The documentation package may be provided in either hard copy or electronic data. All electronic data shall meet the requirements of a standard format such as defined in IPC-2511 or IPC-2581.

Other documentation may include numerical control data for drilling, routing, libraries, tests, artwork, and special tooling. There are design and documentation features/requirements that apply to the basic layout, the production master (artwork), the mounting structure itself, and the end item component or printed board assembly. All must be taken into consideration during the design of the mounting structures for the bare die, or the mounting structure for the BGA.

Documentation shall meet the requirements of IPC-D-325. In order to provide the best documentation package possible, it is important to review IPC-D-325 and identify all the criteria that are affected by the design process.

6.8.1 Drawing Requirements During the formal design review prior to layout, special tools that can be generated by the design area in the form of artwork or numerical control data shall be considered. This tooling may be needed by fabrication, assembly, or testing. Examples of such tooling are artwork overlays, artwork solder resist stripping, numerical data for automatic attachment, solder paste stencil, plots of numerical data to be used as check films.

When viewing the documentation, it is always viewed from the primary side. All phototool generation is viewed from that same direction. The definition of layers of the product

shall be viewed as viewing from and looking through the particular part from the primary side.

Accuracy and skill must be sufficient to eliminate inaccuracies from the layout as being interpreted during the artwork generation process. This requirement can be minimized by strictly adhering to grid systems, which define all features on the board or on the bare die.

Layout notes should be as complete as possible with the addition of appropriate notations. Marking requirements and revision status level definition is key to maintaining configuration management conditions. It is especially important for the engineering review cycle, a quoting effort, and when the document is used by someone other than the originator.

6.8.2 Electronic Data Transfer All information about documentation is also appropriate for electronic data transmission. Since many CAD systems have their own native database, everyone is promoting some form of unique format that has a neutral concept, thus avoiding sending the native database to the suppliers.

Unfortunately, the lowest common denominator for years has been a machine language. This is trying to be circumvented by such formats as the IPC-D-350, IPC-D-356, IPC-2511 or IPC-2581. Archiving electronic data should be in accordance with these documents. Delivery of computer generated data as a part of the documentation package should meet the requirements stated in those packages. With automated techniques, the database shall detail all information that will be needed to produce the printed board or mounting structure for the bare die. This includes all notes, plating requirements, board thickness, etc. The test plots should be employed to verify that the data matches the requirements.

6.8.3 Specifications In many instances, documentation references other specifications. These should be clear and should be provided in this same manner in which the original package is provided (hard copy or electronic). Conformance test circuitry shall be provided, thus the part can be tested through destructive techniques. As a minimum, conformance test circuitry shall include:

- Board part number/revision letter.
- Traceability identification.
- Date code.
- Manufacturer's identification e.g., commercial and government entity (CAGE) logo, etc.
- Special coding systems may be used provided they are identified on the master drawing.

7 ASSEMBLY OF BGAS ON PRINTED CIRCUIT BOARDS

7.1 SMT Assembly Processes The assembly processes for attaching BGA components are more forgiving than the processes for attaching fine pitch peripheral components. Process defect rates can be greatly reduced, however good process control is a necessity.

7.1.1 Solder Paste and Its Application The surface mount assembly process uses solder paste to connect the BGA balls to the land on the board. Solder paste can be applied to the land using three methods: screening, stenciling, and dispensing. BGAs are typically printed using stenciling where solder paste is applied on the BGA land through aperture on the stencil of similar size to the BGA land.

Stencil thickness and aperture size will determine paste volume, which is very critical for ceramic BGAs. The stencil thickness may need to be reduced when using finer pitch BGA components. It is helpful to have trapezoidal stencil apertures (slightly larger opening on the bottom than on the top) for better paste release. Generally, on larger BGA components with 1.25 mm and 1.00 mm pitch, the aperture is large enough that stencil clogging, print registration and definition are less of a problem than with QFP components.

Solder paste consists of a homogeneous mixture of metal powder particles and flux. The metal content (typically 90%) in the solder paste determines the amount of solder in the solder joint. The most common solder paste alloy is the eutectic Sn63Pb37. Metal powder particles are generally spherical in shape. A uniform shape aids the printing or dispensing process and it decreases the surface area, which minimizes oxidation.

Flux and solvents make up the remaining substances in the solder paste. The activators in the flux remove oxides from the solder particles, the land, and the BGA balls. They promote good solderability during reflow process. Solder balls, which form for a variety of reasons during reflow, are a reliability concern, especially when fine pitch devices are involved. The solvents have an important role in controlling the tackiness of the paste and affecting the rheological properties. The formation of voids in the BGA solder joint may be related to solvents in the solder paste. Solvents with low boiling points and/or improper reflow parameters can increase the incidence of voids in BGA solder joints.

For successful fine pitch BGA printing, the solder paste must pass through very small apertures on the stencil. The solder paste needs to remain printable and tacky for an extended period of time, and it must maintain print definition prior to and during reflow. Solder paste viscosity, particle size and stencil life are critical parameters for solder paste application.

7.1.1.1 Particle Size and Paste Selection Many solder pastes are available and one should be selected based on the print characteristics, flux type, and fine pitch particle

size. First of all it is important that the solder paste print well, providing good print definition without exhibiting solder paste slump. The flux in the paste must be active enough to exhibit good wetting and reflow characteristics, yet it must be compatible with the cleaning process or surface resistivity requirements. It is important that the diameter of the particle size does not exceed the aperture width divided by 4.2, determined through empirical experimentation. When this rule is violated the paste release and print definition are affected.

The solder particle size is classified by J-STD-005 (see Table 7-1).

Table 7-1 Particle Size Comparisons

Solder Paste Type	Mesh	Maximum Particle Size [in μm]
Type 2	-200/+325	75
Type 3	-325/+500	53
Type 4	-400/+500	38
Type 5	-500	25

Particle size distribution affects the solder paste viscosity and printability. Type 3 paste is the most commonly used, and it is adequate for most printing applications. Ultra fine pitch CSP application may require Type 4 paste.

7.1.1.2 Stencil Thickness and Aperture Design As is the case for all components, as the pitch of the part decreases it becomes necessary to decrease the stencil thickness. For BGA components in the range of 1.5 mm to 1.0 mm a stencil can range from 0.15 to 0.18 mm thick. For chip scale packages (CSP) or fine pitch BGAs with a pitch equal to or less than 0.80 mm a stencil thickness range of 0.1 to 0.15 is recommended.

It is very important to design a stencil aperture that will provide good paste release. In order to insure good paste release, an aspect ratio of 1.5 is recommended. Aspect ratio is the ratio between stencil aperture width and stencil thickness. When printing small round apertures for finer pitch BGAs the area aspect ratio must be taken into account. An area aspect ratio of greater than 66% is recommended. The formula to calculate area aspect ratio is the length times the width/2 (length plus width) times stencil thickness.

$$\frac{LxW}{2(L+W)} \text{ x } T$$

i.e., a square aperture with a dimension of 0.35 mm with a stencil thickness of 0.125 mm gives the resulting aspect ratio:

$$\frac{0.35x0.35}{2(0.35+0.35)x0.125} = \frac{0.1225}{0.175} = 0.70$$

Using an overprint or an aperture larger than the land may be necessary to achieve this ratio, and is desirable to provide a larger target for placement. This feature also provides for greater adhesion of the component to the land on the mounting structure prior to reflow. An overprint of 50 µm to 75 µm larger than the land for fine pitch BGAs is recommended. A square aperture with rounded corners will also provide better paste release and volume deposition.

For CBGA components where thicker solder volume is required, a stepped stencil may be used. The step is typically 0.04-0.08 mm, and it can put two different paste thicknesses on the board surface. Usually a rubber squeegee is preferred when stepped stencil is used, but a metal squeegee can be used successfully when the step is 0.04 mm. If a stepped stencil is used, the step line should be at least 3.75 mm away from any print aperture.

7.1.1.3 Importance of Paste Volume For plastic BGAs much of their solder volume is supplied by the solder ball on the part itself and the paste volume is not all that critical. For BGAs above 0.80 mm pitch, stencil thickness will be dictated by the other component types used on the printed board assembly. Solder volume and stencil thickness become more critical for ceramic and fine-pitch BGA such as CSP. The solder balls used on ceramic BGAs are not eutectic and do not collapse during the reflow process (see Figure 7-1).

Because the high lead content ball does not collaspe having sufficient solder paste is critical. The fillet between the land and ball depend upon the solder paste volume. Ceramic BGA requires a minimum of 0.08 cubic mm and a nominal 0.12 cubic mm paste volume.

In order to achieve 0.12 cubic mm of solder paste, it may be necessary to overprint with a 0.2 mm stencil. For other components on a circuit board with CBGAs, the aperture size may need to be adjusted to compensate for the thicker stencil or it may be necessary to step the stencil.

7.1.2 Component Placement Impact Getting into BGA technology also requires some new assembly capability. Depending upon the type of pick and place systems, a change in package carrier mechanism may also be required to transfer packages from matrix tray to the pick position. Fiducials may also be helpful in helping the vision systems reorganize the exact location of the land pattern for the BGA, similar to what is used for fine-pitch peripheral leaded parts. Large BGA parts on tape-and-reel will require 44 mm and 56 mm feeders depending on the body size.

7.1.3 Vision Systems for Placement Placement accuracy is a very critical part of the BGA process. Unlike some surface mount components it is not advisable to move a BGA by hand to correct placement problems. The placement machine's accuracy is largely dependent on the vision system and the ability of the nozzle to hold the component. Matching the vision system to the application

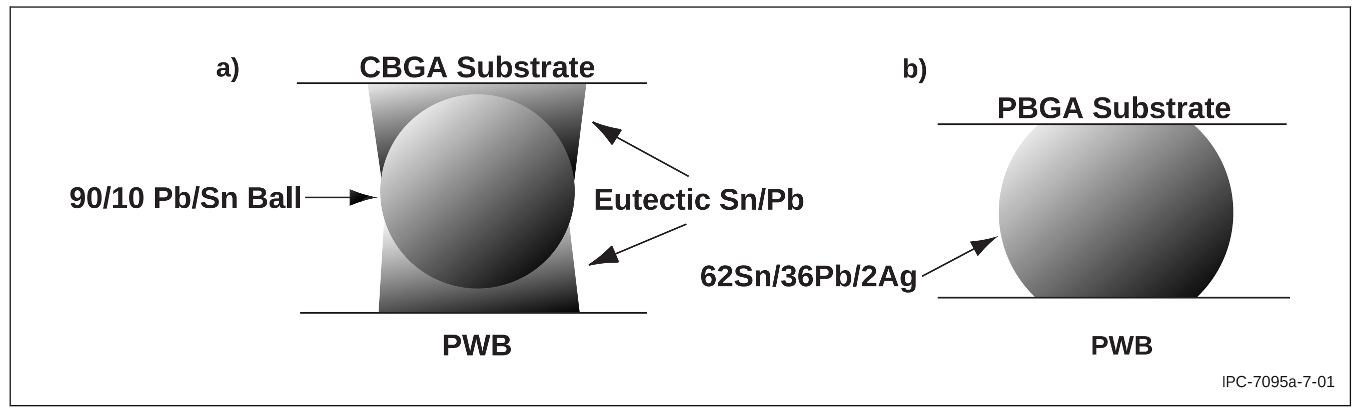


Figure 7-1 High Lead and Eutectic Solder Ball and Joint Comparison

is also important. The vision system determines the X, Y and theta offset of each component prior to placement. In addition to determining the component offset, the vision system can also inspect the component for dimensional integrity. CCD camera based systems employ two lighting methods, referred to as binary and gray scale. Both methods can be sensitive to contrast and lighting changes.

Gray scale systems use front lighting, which illuminates the component from below. Surface features are reflected into the CCD camera for processing. Binary systems use back lighting, which illuminates the component from above. The outline of the component is projected into the CCD camera for processing. Binary imaging, which is the older of the two methods, locates a feature using the contrast between black and white images. Gray scale systems can usually interpret 256 levels of contrast. Both systems use an algorithm to determine the center of the component. Binary imaging requires less computing capability than gray scale imaging.

Gray scale imaging places BGA components based on ball location while binary imaging places BGA components based on the component outline. In some cases the tolerance between the BGA outline and the balls is significant. Gray scale imaging is more desirable for placing BGA components because it eliminates placement error due to variations in the component outline.

Placement machine nozzle designs vary from supplier to supplier. It is important that the correct nozzle is chosen which will have sufficient surface area to hold the part without any shifting during the placement process. The nozzle must gasket against the part not allowing vacuum leakage. Tactile sensing, which helps control the Z axis (vertical) stroke of the spindle, is desirable because it prevents a component from being crushed between the vacuum nozzle and the substrate.

7.1.4 Reflow Soldering and Profiling Reflow soldering is a complex process with many variables. All mass reflow systems incorporate convective, conductive and radiant means of heat transfer, to what degree depends on the design of the reflow system. All designs strive to achieve the same fundamental results. Five different phases take place during reflow. The five phases are: (1) evaporate solvents from the solder paste, (2) activate the flux and allow fluxing action to occur, (3) preheat the components and printed circuit board, (4) melt the solder and allow proper wetting to occur, and (5) cool the soldered assembly.

Over the years, reflow equipment has changed frequently. Four design concepts have been used: vapor phase, lamp infrared (IR), panel IR, and most recently, forced gas convection. Vapor phase reflow technology evolved first and was popular for a few years. Eventually, IR became the preferred approach. In the early 1990s, forced gas convection technology was introduced, and today, it is the method of choice.

7.1.4.1 Forced Gas Convection Heat is transferred to the printed circuit assembly (PCA) by low velocity heated gas. Forced gas convection is a contact heating method, with some heating accomplished by radiation. The rate at which heat is transferred to the object is directly proportional to the difference in temperature between the heated gas and the PCA.

Inline forced gas convection systems have three main sections: (1) preheat, (2) reflow and (3) cooling. Each section contains a number of top and bottom zones. The number of zones has a direct effect on the transport speed and the user’s ability to fine tune the profile. Adding more zones allows the user to run a faster transport speed and it permits more accurate profiling. Low volume reflow systems have three or four zone sections (a zone section includes top and bottom heaters). Medium volume reflow systems have five or six zone sections, while the higher volume systems use seven or more. Typically, a six zone system will satisfy most reflow requirements, including very large PCAs and reasonably high transport speeds (up to 60 cm per minute). Profile changes are accomplished by adjusting the transport speed and top and bottom temperature settings.

7.1.4.2 Time/Temperature Profiles Many factors influence a reflow profile, including the solder paste, the substrate and the components. A common reflow profile is shown in Figure 7-2. This profile produces a continuous, gradual ramp up and ramp down. As described earlier, the reflow process has three phases. The preheat phase is the preparatory phase. All actions leading up to proper reflow occur during preheat. The reflow phase occurs when the temperature of the solder and the solderable surfaces are above the melting temperature of the solder alloy. This elevated temperature promotes proper solder wetting. The cool down phase helps control the dwell time and provides the proper cool down rate for the solder joint.

Profiling should be thought of as a range rather than a single point. If the cycle time parameters for proper reflow are added up the reflow cycle time should range between three and four minutes. This information can be used to calculate transport speed. To calculate the transport speed divide the heated oven length by 3 (maximum speed) or 4 (minimum speed). For example, if the heated length is 183 cm, then the conveyor speed range is 46 to 61 cm per minute. A unique feature of forced gas convection is the ability to reflow hundreds of different boards with a few (3 to 6) reflow profiles.

7.1.4.3 Material Issues Printed circuit boards (PCB) can be damaged by excessive or extended exposure to heat. The Glass Transition (T_g) temperature of the PCB material must be known to help create the reflow profile. Standard laminates have a T_g around 130°C. High temperature laminates, with a T_g around 170°C, are also available. Two damaging things can occur above T_g. The material becomes plastic, so the PCB becomes soft and loses its rigidity. Also, the expansion rate of the material increases dramatically, which can damage the plated-through holes by cracking the barrel.

Flux has two key attributes. First, it must remove contamination and second, it must protect the solderable surfaces after contamination removal. A common mistake is to use a time/temperature profile that consumes the flux before the solder melts. Ideally, the flux would be consumed just as the solder begins to melt. Activation time should range from 90 to 120 seconds. Flux usually becomes active at around 130°C.

Components can be damaged by the incorrect application of heat. All components have a heat exposure limit. Most surface mount components should tolerate a peak temperature of 220°C for up to 60 seconds. Thermal shock, caused by the rapid application of heat, can crack certain components. However, since the peak temperature of reflow ovens varies, the intent is to heat the solder to a solder joint temperature of 210°C to 220°C.

Component lead finish will affect solderability. There are a number of lead finishes being used today, including tin/lead, gold, tin and palladium. It is important to select a flux

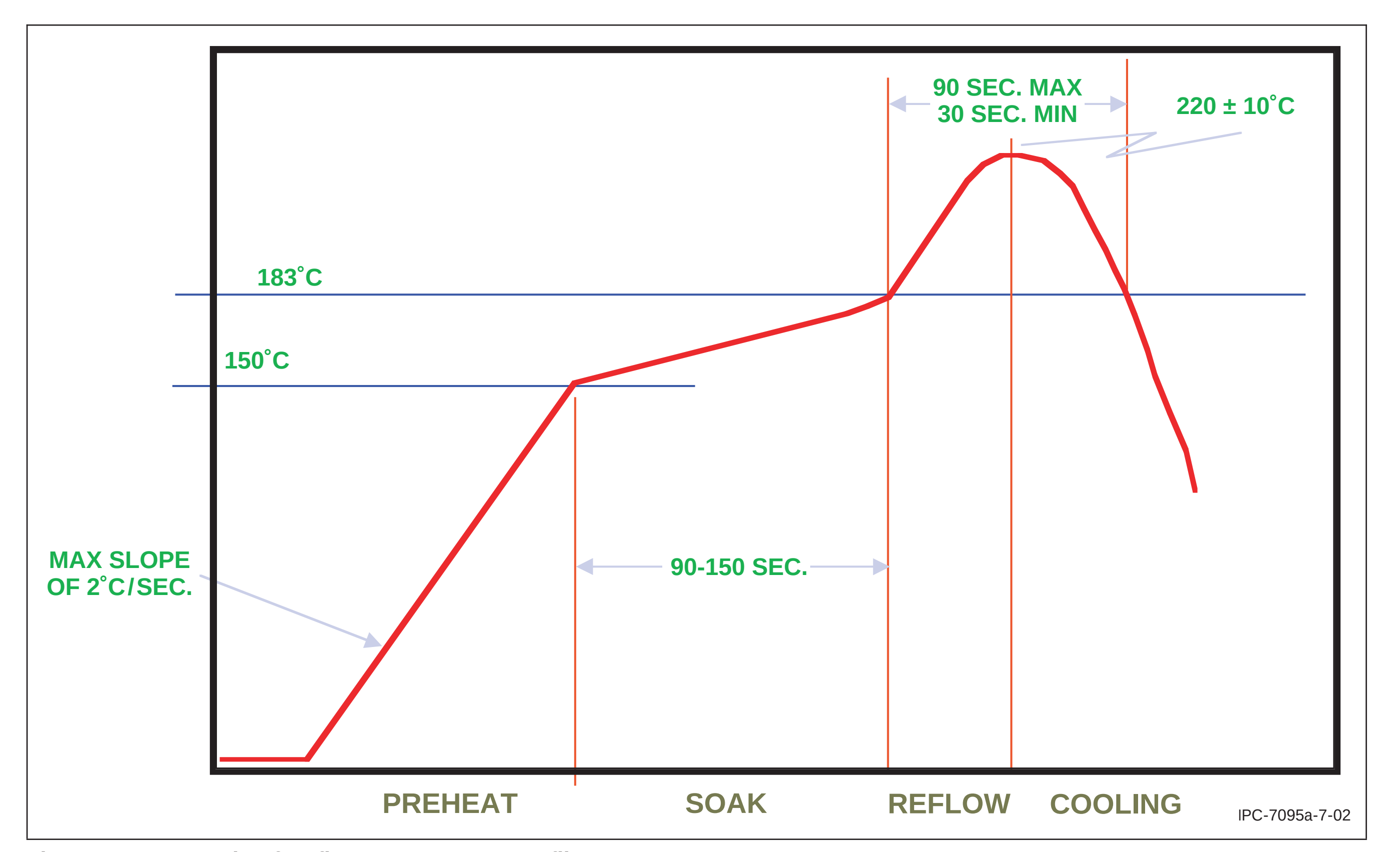


Figure 7-2 Example of Reflow Temperature Profile

and solder alloy that works well with the lead finish being used.

The solder alloy should be heated to a temperature that is 25°C to 40°C above its melting temperature. The dwell time above the melting temperature should be 30 to 90 seconds. Solder and organic coated boards typically require a dwell time of about 60 seconds. Nickel gold coated boards typically require a dwell time of about 90 seconds. Proper reflow temperature and dwell time permit proper wetting to occur (see Figure 7-2).

7.1.4.4 Vapor Phase Vapor phase reflow can be operated as a single fluid system or a two fluid system, utilizing a primary and a secondary fluid. The process was developed using the two fluid approach in batch equipment; but modern in-line systems are normally operated with only one fluid. Whichever system is used, the maximum temperature reached by assemblies in vapor phase (VP) reflow depends on the choice of the primary fluid. Primary fluids are available in a number of temperature ranges, with 218°C to 222°C being common.

While all the primary fluids can be classed as perfluorocarbons, the basic structure (amine, cyclic or ether) will determine the key properties of in-use stability, solder paste chemicals solubility and overall process economics. The choice of a fluid is normally based on the melting point of the solder alloy to be reflowed.

For the range cited, the lower temperatures are suitable for the typical tin-lead or tin-lead-silver alloys used for standard attachment processes. The upper end of the range will permit reflow of high lead alloys, which are used to attach pins to PGA packages. Users faced with reflow of a specialty alloy have been successful in mixing two primary fluids to tailor a VP system for a specific stable boiling point. Higher temperatures will permit shorter times, which may be advantageous with some solder pastes.

The primary vapor phase should be inert and not introduce contaminants that must be removed later. Solder paste chemicals that dissolved in the fluid are carried in the high boiling vapor then deposited on the surface of the boards. Such residues tend to be difficult to remove. Minimizing solder paste residue in the primary fluid will maximize the lifetime of the fluid, prevent boiling point elevation due to dissolved paste ingredients and simplify cleaning.

The secondary vapor blanket was originally CFC-113, a lower boiling fluorinated material, which formed a low cost sacrificial ‘‘lid’’ over the more costly primary fluid. The constant exposure to the high boiling primary fluid at the interface of the two fluids could cause the secondary fluid to undergo thermal decomposition at the interface, generating HCl (hydrochloric) and HF (hydrofluoric) acid vapors. These corrosive vapors often attacked the soldering equipment over time. While in theory the vapors could be absorbed in flux residues and cause problems for high reliability products, this was rare in comparison to the attack on the equipment. With the phase out of CFC-113, a low boiling perfluorocarbon was introduced to replace it. This second generation secondary blanket fluid was more stable than CFC-113 for prolonged exposure to the high boiling vapor phase fluids.

As surface mount technology grew, most users converted to the higher throughput in-line machines, which used the single fluid approach. Defluxing after vapor phase reflow should be done with either a bipolar solvent formulation or include an aqueous cleaning formulation that can ensure removal of all the solder paste residues, with the choice of cleaning process based on the composition of the solder paste. Secondary factors influencing the decision would be compatibility, and the component to PWB surface spacing.

7.1.5 Cleaning Vs. No-Clean The selection of a particular cleaning process depends on the types of contaminant present, and these are determined by the type of flux and by the soldering and handling methods. Generally, for reflow soldered surface mount assemblies, rosin, organic acid, and no-clean fluxes are used. For wave soldering of either mixed or through-hole mount assemblies, no-clean, rosin, and water-soluble fluxes are used. The water-soluble fluxes require water for cleaning, whereas the rosin fluxes are generally cleaned with semiaqueous and organic solvents. Selection of a cleaning solvent should follow a careful evaluation of technical, economic, and environmental considerations.

In general, cleaning surface mount assemblies is more difficult because the tight gap between the board and components may entrap flux which may be difficult to remove during cleaning. However, if proper care is taken in selecting the cleaning processes and equipment, and if the soldering and cleaning processes are properly controlled, cleaning surface mount assemblies should not be an issue even when aggressive fluxes are used. It does need to be emphasized, however, that good process control is essential when using aggressive water-soluble fluxes. When no-clean fluxes are used, boards do not require cleaning, of course, but the stencils should still be cleaned to ensure good printing. Both semiaqueous and aqueous solvents work well for stencil cleaning. The use of no-clean fluxes is increasing due to the environmental concerns of using fluxes that require cleaning and the disposal of used solvents containing lead. However, no-clean is not a drop-in process. To be effective, it requires a change in company culture and will impact not only the internal operation but the operations of the suppliers as well.

No-clean flux is not as active as other types of flux and hence the soldering results may be less than desired unless adequate steps are taken. The use of relatively active flux

helps improve the soldering yield, but the flux residues must be cleaned and the used solvents must be properly disposed of.

It must be noted, however, that there is no such thing as the ideal flux, the ideal cleaning method, or the ideal method for determining cleanliness. These variables depend on the application. The user must establish requirements for flux, cleaning and cleanliness testing based on empirical data for a particular application.

7.1.6 Package Standoff Package Standoff for a BGA is defined as the distance between the land on the bottom of the package substrate and the land on the top of the board surface. This distance varies depending on the type of solder ball: the high lead ball type stays a fairly consistent size; the eutectic solder ball reduces the package standoff height. This is also known as Ball Collapse Height. When the BGA is soldered on the board, the balls ''collapse'' during reflow and reduce the package standoff by 0.25 to 0.30 mm less than the pre-reflowed value. The high lead balls do not collapse.

Factors that determine the post-reflow BGA package standoff from the board include the BGA package weight, the ball size, the ball material, the land size and land configuration (solder mask defined or nonsolder mask defined).

Standoff height decreases with increased package weight. However, for packages with a large ball count, the package weight may have less effect on the standoff height. One study on the relationship between these two parameters discovered that increasing the package weight by 5X decreased the standoff height by only about 0.05 mm for a 615 ball, 1.27 mm ball pitch BGA package.

Larger ball sizes will lead to larger package standoff heights due to the larger volume of solder in each ball. Standoff heights are inversely proportional to the land diameters. For nonsoldermask defined (NSMD) lands, a soldermask relief around the land may reduce the standoff height, because the solder will wet out along the conductors as well as along the edges of the land. This is shown in Figure 7-3.

7.1.7 Equipment Messaging Protocols Throughout the electronics industry manufacturing consists of numerous steps, each of which often centers around one supplier's equipment. Although the steps are generally well-automated within themselves, they only peripherally connect to one another. Proprietary data formats and communications protocols prevent the islands of automation from talking to one another. This condition also prevents factory managers from monitoring, understanding, and possibly

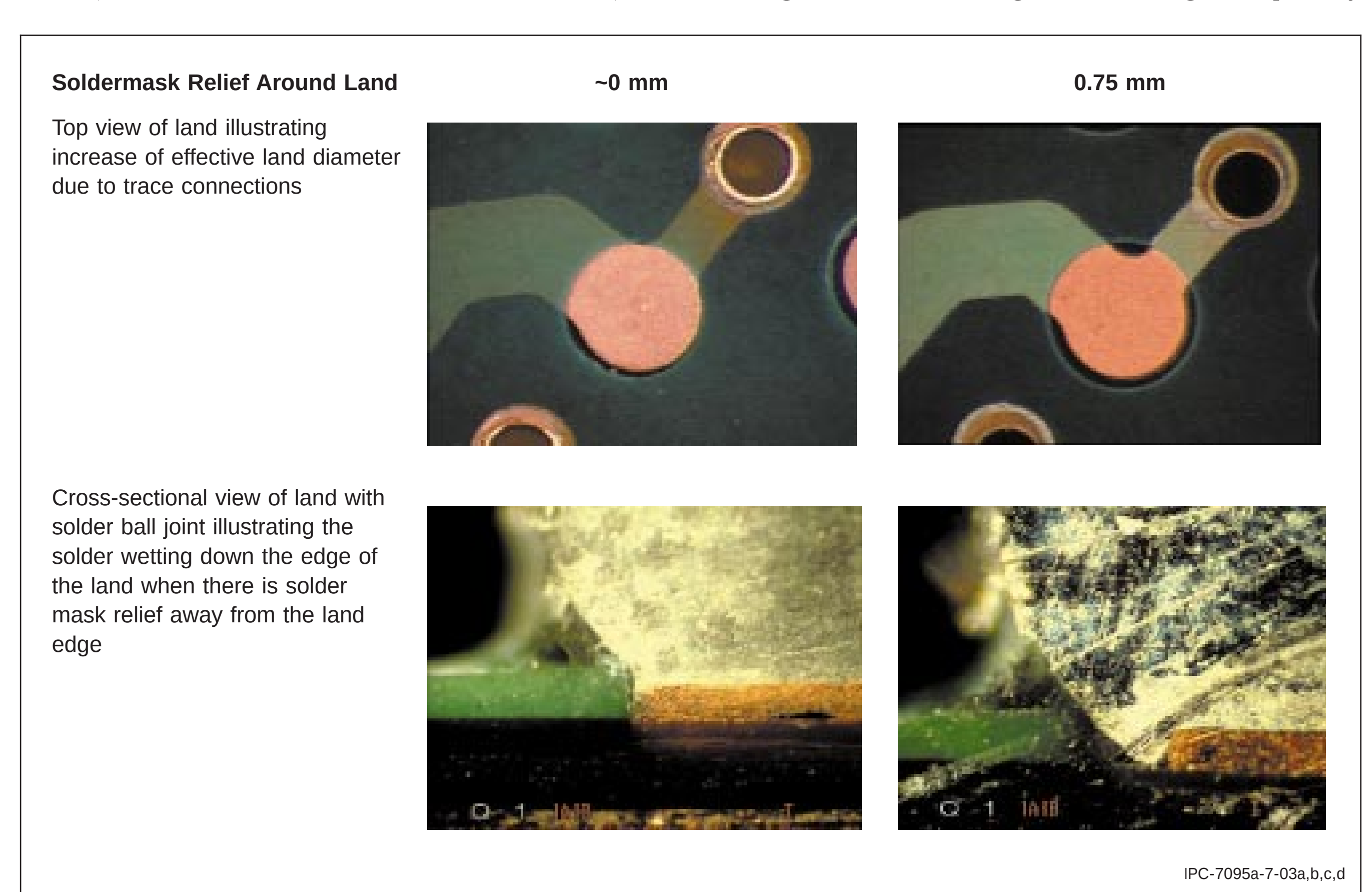


Figure 7-3 Effect of Having Solder Mask Relief Around the BGA Lands of the Board

correcting the manufacturing process to improve throughput and product quality.

In the last few years building on a National Electronics Manufacturing Initiative (NEMI) funded a project the IPC has standardized data syntax and semantics in electronics assembly, establishing rules for data exchange both on a single factory floor and between that floor and the rest of a manufacturing organization. The results have been published as the IPC CAMX (computer-aided manufacturing using the extensible markup language [XML]) standards: The standards are:

- IPC-2541 *''Generic Requirements for Electronics-Manufacturing Shop-Floor Equipment''*
- IPC-2546 *''Sectional Requirements for Specific Printed-Circuit-Board Assembly Equipment''*
- IPC-2547 *''Sectional Requirements for Electronics Manufacturing Test, Inspection, and Rework Station Communications''*

At the heart of the standard is a framework with an intermediary. This is the ''message broker'' that handles information exchange and complies with the IPC-2501 Standard (''Definition for Web-based Exchange of XML Data''). The message broker can be thought of as a post office or a mail server. Messages are sent to the server and when the information is needed it is asked for by the equipment or the manager who wants the data.

In a factory, several lines of equipment and several applications may connect to the message broker at the same time. Individual elements need not know any details about the nature, configuration, or format of the others. They communicate directly only with the broker. When people and equipment need specific information, the broker provides it in the correct format.

7.1.7.1 Implementation It is relatively easy to set up the infrastructure and Web-based tools to monitor several sets of manufacturing equipment, including in-circuit testers, and several suppliers' pick-and-place machines. The setup can be used to gathered performance and functional feedback data on the message broker. The message broker can usually be up and running in two days, being able to connect reasonably easily with both legacy equipment and any XML-ready equipment using an infrastructure that is in place at the manufacturing site. In a careful installation, it is also possible to avoid compromising network security requirements.

Using internet standards like HTTP and XML ensures the interoperability between different platforms. Although an application has never been run against a running message broker before, it can be adapted to the existing communication framework on site. One important goal of the IPC CAMX standards is to lower the technological barrier to ease the integration of sophisticated equipment like pick-and-place machines and test equipment, as well as simpler equipment like printed board handlers.

The CAMX standards provide data about the products under manufacture, the processes, and the shop-floor equipment. Applications receiving messages from the equipment include:

- Work-in-process (WIP).
- Tracking, capacity, and throughput monitors.
- Equipment utilization and line-balancing monitors.
- Product quality monitors that incorporated data from test and inspection.

Linking all parts of a manufacturing operation through a single hub has been the goal for many years. The CAMX message-broker approach provides an extraordinary array of tools to accomplish that task. The message broker can connect any number of clients together. Clients can be factory equipment, a host computer, or the data hub at the engineering manager's desk. The system provides visual representation of whatever the manager wants to know. The manager can communicate with someone in Singapore, and check the status of their work-in-process using a snapshot of the data in any of a number of preset formats. He can pick the format and instruct the software as to how frequently the updates are required, and the broker does the rest.

7.1.7.2 Information Exchange Benefits Major equipment manufacturers have involved themselves in this effort from the beginning, thus they support the CAMX effort to extract information from their machines in the standard format. Critical to the success of this new tool is its ''plug-and-play'' construction. Any piece of equipment on the floor can connect to the supporting architecture and data-gathering software. Using XML as the standard ensures that no one will misinterpret what the data means. Process correction and product improvement require *traceability* of faults, regardless of where a fault is identified. Knowing where the fault came from and its root cause are critical.

In addition, increasing product quality and reducing costs require understanding the actual fault spectrum. Historically, the same fault may be called by several names at different process points. Applying the CAMX standard, fault names can be consistent from step to step within the manufacturing operation, thereby improving the overall level of communication.

For electronics manufacturing-service (EMS) providers, the CAMX standards permit manufacturing flexibility without sacrificing data coherence and comprehensive data analysis, regardless of the process under evaluation. The software is more streamlined and less complex than systems that were developed for the semiconductor industry because all of the equipment now conforms to the single

standard. The result is equipment that is both easier to use and easier to support.

Standardization will open up opportunities to perform more elaborate data analysis because the standards will reduce the effort required to gather information. IPC-2501, as implemented in the CAMX message broker, provides the simplified Web-based XML messaging activity for the other IPC standard vocabularies. Equipment suppliers who need a particular piece of information will merely ‘‘subscribe’’ to an application or system using the existing Web-based and universal XML messaging SOAP protocol, regardless of the architecture of the other interfaces, and download responses in real time. SOAP is an XML messaging standard supported by all major computing and software vendors. It forms the foundation of their Web-services infrastructures.

The type of machine communication was less necessary when OEMs did their own manufacturing. However, with the amount of outsourcing that kind of vertical integration has become more the exception than the rule. The new standards will make it possible for the OEM customer to regain a measure of the insight into manufacturing activity that was lost due to outsourcing the work.

The use of a universal data format will also provide the ability of suppliers to monitor inventory of their products to prevent disruptions of the manufacturing line. Component suppliers can monitor usage of their components on the factory floor, scheduling purchases and taking over similar functions that otherwise fall to the EMS company or to the OEM.

7.2 Post-SMT Processes

7.2.1 Conformal Coatings Conformal coatings are used to protect the parts from surface moisture and thus corrosion. Conformal coatings should be specified to meet the requirements of IPC-CC-830 and should be specified on the master assembly drawing. When UL requirements are imposed, the coatings shall be approved by UL for use by the printed board manufacturer.

The designer should be cognizant of compatibility issues. Conformal coating is an electrical insulation material which conforms to the shape of the circuit board and its components. It is applied for the purpose of improving surface dielectric properties and protecting them from the effects of a severe environment. Conformal coatings are not required on surfaces or in areas that have no electrical conductors.

Conformal coatings may be any of five types. The thickness of the conformal coatings shall be as follows for the type specified:

- AR – acrylic resin, 0.03 - 0.13 mm
- ER – epoxy resin, 0.03 - 0.13 mm
- UR – urethane resin, 0.03 - 0.13 mm
- SR – silicon resin, 0.05 - 0.21 mm
- XY – paraxylene resin, 0.01 - 0.05 mm

There are three primary chemical categories in use for conformal coatings. These are silicon elastometers, organics, and parylene. All three types provide various levels of protection from solvents, moisture, corrosion, arcing and other environmental factors that can jeopardize the circuit operation.

Conformal coatings may also be used in greater thicknesses as shock and vibration dampening agents. This type of application brings with it the risk of mechanical stress to glass and ceramic-sealed parts during cold temperature excursions. Using this material may require the use of buffer materials.

Conformal coating should not be confused with encapsulants. Encapsulants are used primarily to protect the bare die as a part of the chip component package. Plastic encapsulants provide the protection of the plastic BGA from external sources. The compatibility issues of encapsulants and thermal coatings are very similar.

7.2.2 Depaneling of Boards and Modules For printed board routing, it is recommended that the number of cutouts and notches be kept to a minimum to decrease the amount of fabrication time. Cutouts and notches should allow for a minimum radius of 1.5 mm on internal corners (assuming that a 3 mm diameter router bit is used). Although minimum internal radius of 0.75 mm can be obtained with a 1.5 mm diameter router bit, this requirement should be avoided as router efficiency and accuracy decreases substantially when smaller router bits are used.

Recommended tolerance for the location and profile cutouts and notches are shown in Table 7-2, however the tolerance specified on the printed board drawing should accommodate the dimensions. Frequently, a combination of routing and scoring is used.

Table 7-2 Tolerance of Profiles, Cutouts, Notches, and Keying Slots, as Machined, mm

Tolerances to be Applied to Profile of a Surface	Level A	Level B	Level C
Profile feature	0.25	0.20	0.15
Location where greatest basic location dimension is less than 300.0	0.30	0.25	0.20
Location where greatest basic location dimension is greater than 300.0	0.35	0.30	0.25

The final method involves the use of routing and drilling break away tabs (see Figure 7-4). Panelization of parts is a

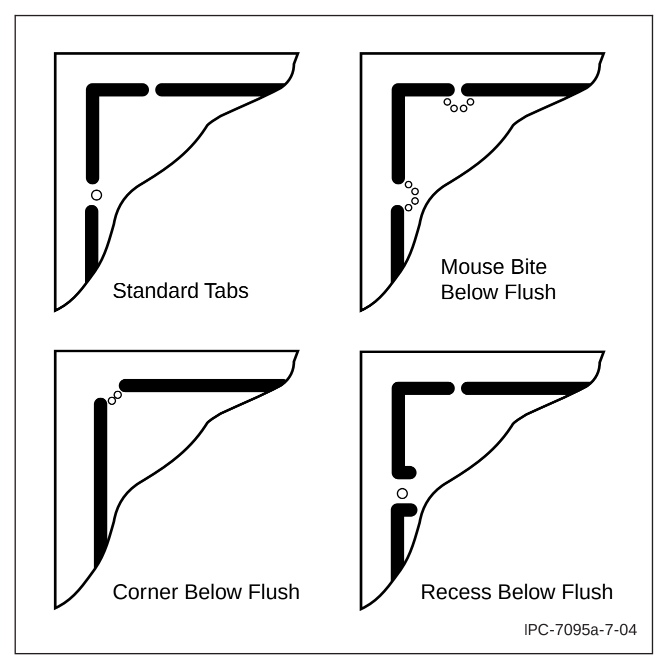


Figure 7-4 Breakaway Tabs

standard process in many instances for both test and assembly. This can be achieved using a number of different techniques. These include simple scoring, a combination of routing and scoring, and a combination of routing plus breakaway.

Scoring is the machining of a shallow, precise V-groove into the top and bottom surfaces of the laminate. It is generally accomplished using CNC equipment. As scoring allows the removal of rails and individual parts from a pallet, positional accuracy is critical. (See Table 7-3 and Figure 7-5 for some standard scoring parameters.)

Extreme care should be taken when break away tabs are removed. Avoid bending the board, especially near BGA components. Bending may cause BGA solder joints to crack, typically starting with the corner balls. Custom tools should be fabricated or machines designed for break away

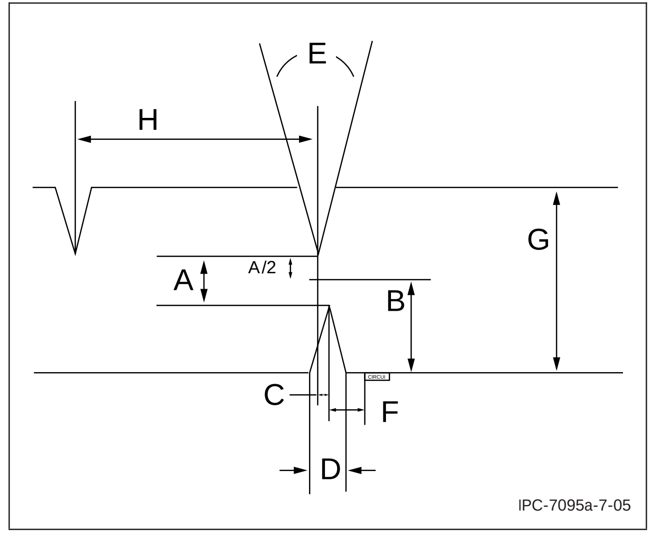


Figure 7-5 Standard Scoring Parameters

tab removal should be purchased. These tools or machines should reduce or eliminate stress near BGA components during break away tab removal.

7.3 Inspection Techniques The following paragraphs are inspection techniques that may be applied at different times during the development of the BGA assembly process or as an auditing mechanism during production. Table 7-4 provides some recommendations as to applicability of the inspection method.

7.3.1 X-Ray Usage X-ray inspection is generally used when there is a high proportion of ‘‘hidden’’ solder joints that are not visually accessible, and when there are a significant number of untestable solder joints. Examples of untestable solder joints are redundant connections, and back-to-back BGAs where the fanout vias are inaccessible and space does not allow for additional test points. X-ray methods can complement the test process chosen, and can provide faster feedback to the manufacturing line. Depending on the capability of the X-ray system being used, X-ray

Table 7-3 Standard Scoring Parameters

Detail Letter	Title	Definition	Attainable Tolerances
A	Web	The material remaining between the two (2) ’V’ scores on a plane perpendicular to the printed board surface	± 80 µm
B	Centrality	The distance the center of a web is offset from true center within the printed board.	± 80 µm
C	Blade Offset	The distance the top and bottom scoring blades are offset from one another.	± 80 µm
D	Score width	The width of a score line at the surface of the printed board	± 80 µm
E	Cutter angle	The total angle of a scoring blade.	± 2°
F	Keep out area	The area, expressed from nominal score line placement, that no features should be placed within.	D/2 + All registration
G	PCB thickness	Overall printed board thickness to be scored.	Per IPC standards
H	Trueness/Position	The tolerance of two or more score lines on one side of the printed board. Measured from nominal, squareness and actual position.	± 80 µm cumulative

Table 7-4 Inspection Usage Application Recommendations

Method	Process Development	In-Line Production	Failure Analysis	Process Auditing	NPI or Low Volume Production
Optical Inspection	Excellent	Good	Excellent	Good	Good
Manual X-ray	Excellent	Good	Excellent	Good	Excellent
Automated Transmission X-Ray	Excellent	Excellent	Good	Good	Good
Automated Cross Section X-Ray	Excellent	Excellent	Excellent	Good	Good
Scanning Acoustic Microscopy	Excellent	Fair	Good	Good	Fair
Stand Off Measurement	Fair	Fair	Good	Good	Fair
Automatic Optical Inspection	Solder paste volume	Part identification, solder paste volume	Not Applicable	Part identification, solder paste volume	Part identification, solder paste volume
Destructive Analysis	Good	Poor	Excellent	Fair	Fair

is capable of detecting solder related defects such as bridging, open solder joints, insufficient solder, and excessive solder volume. Other defect types such as missing balls, misregistration, and package ''popcorning'' can also be identified. In addition to defect detection, X-ray can be used to provide trend analysis for solder volume and solder joint shape. X-ray is the only nondestructive method of finding voids in BGA joints.

Figure 7-6 shows the principles of x-ray equipment being used in an inspection process. The general characteristics provided in the figure apply to most x-ray systems.

X-ray inspection has become a generally accepted tool for solder joint evaluation and analysis, and as a monitor for the reflow process. X-ray inspection techniques can be employed most effectively through the understanding of principles of x-ray image acquisition.

X-ray can be effective in confirming solder bond integrity of BGAs and as a monitor for the reflow process. X-ray inspection techniques can be employed most effectively through the understanding of:

• Principles of x-ray image acquisition

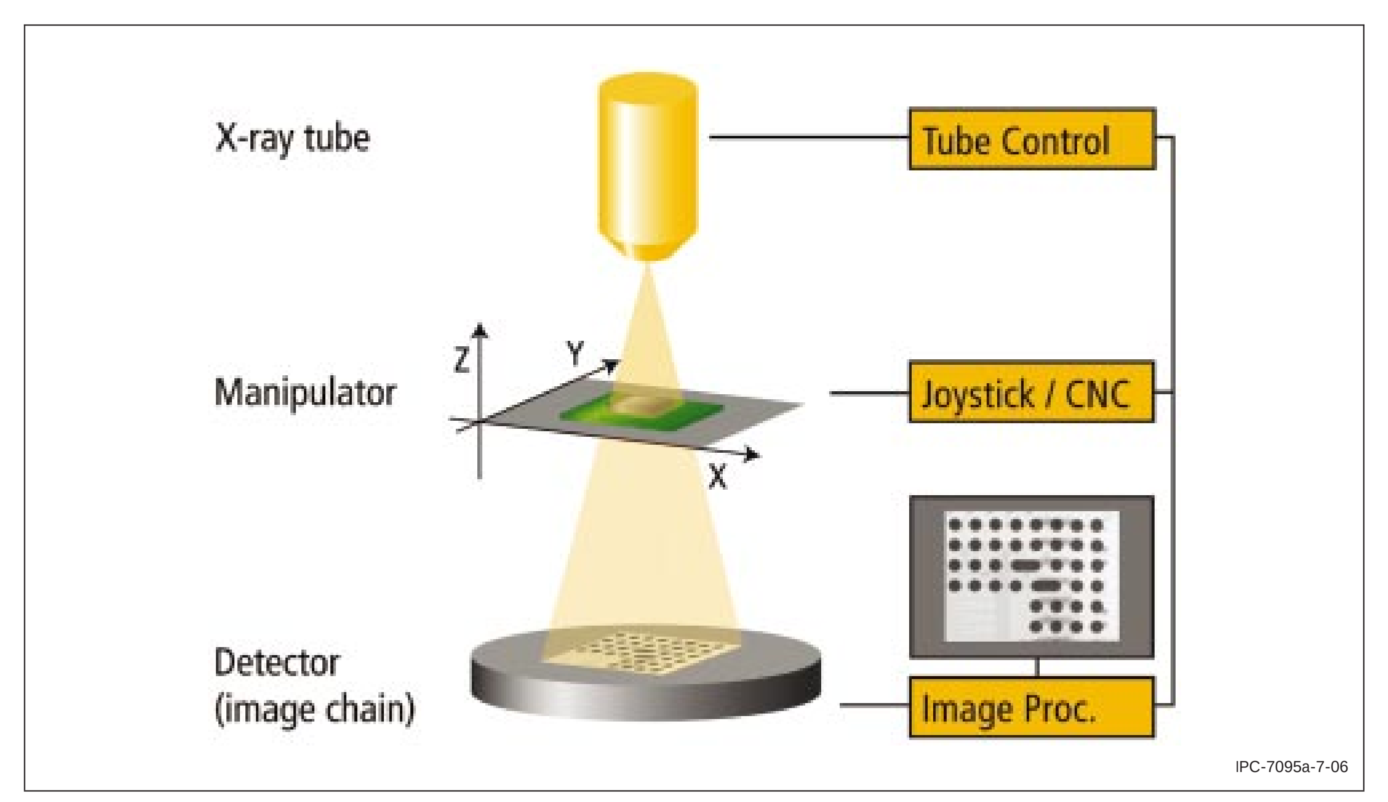


Figure 7-6 Fundamentals of X-Ray Technology

- Analysis of the x-ray image (in the light of the reflow process)

Use of x-ray requires some caution regarding overexposure on vulnerable materials or components.

Figures 7-7 and 7-8 show the characteristics of x-ray images for both voids at the interface, or missing solder balls in the BGA attachment.

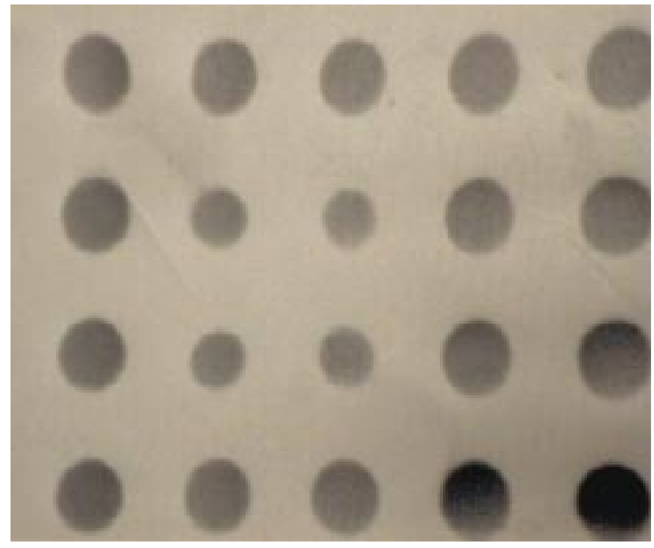


Figure 7-7 X-Ray Example of Missing Solder Balls

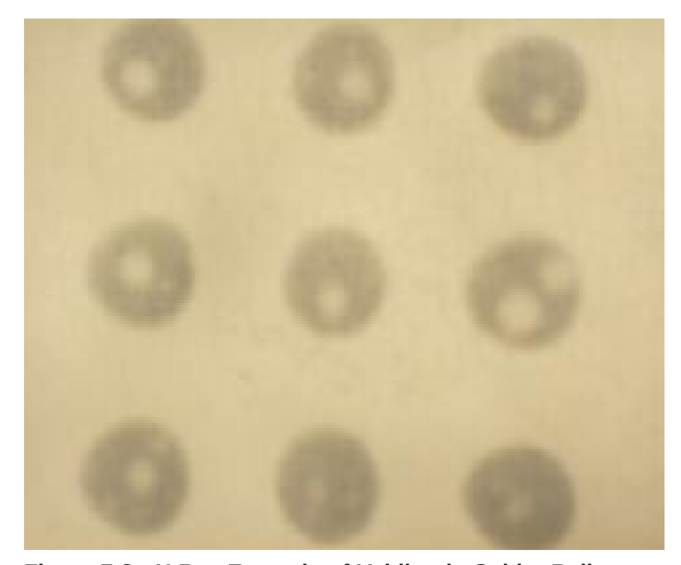


Figure 7-8 X-Ray Example of Voiding in Solder Ball Contacts

7.3.2 X-Ray Image Acquisition

Film Based X-Ray Inspection – Film based x-ray inspection systems employ an industrial x-ray cabinet and x-ray film packets to record the x-ray image on film. The film can then be viewed on video film viewers for high magnification examination of details. The process is slow but can yield x-ray images of great detail and tonal accuracy.

Real Time X-Ray Systems – Real Time x-ray inspection systems utilize an x-ray source and a detector system which converts the invisible x-ray image into a video display signal. These systems provide immediate imaging results of samples. The images produced from these systems should not be distorted or include false artifacts induced by the x-ray system itself. Figure 7-9 illustrates a comparable level of image quality that should be expected from a manual x-ray inspection system. Figure 7-10 illustrates examples of pin-cushion distortion and voltage blooming.

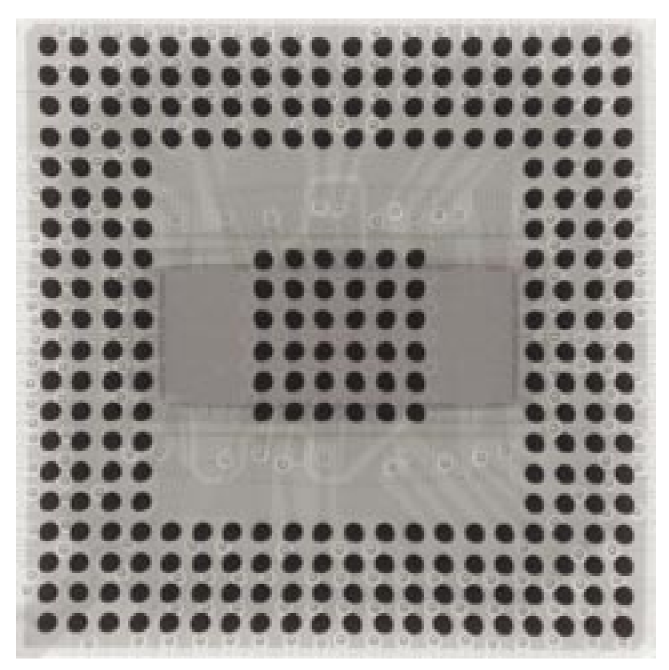


Figure 7-9 Manual X-Ray System Image Quality

Real time systems are available in a broad range of sizes from small desktop systems to large console floor models. They are also available with a broad range of x-ray source voltages. There is not a specific voltage needed to inspect BGAs. The voltage required will, in part, depend on the sensitivity of the particular x-ray system employed, as well as the structure and characteristics of the BGA under inspection. BGAs with copper heat sinks for example, will require higher penetrating voltage settings than PBGAs or CBGAs. BGAs with aluminum heat sinks, on the other hand, do not require the higher voltages since aluminum is a less dense material and is therefore much more transparent to x-rays than copper.

7.3.3 Definition and Discussion of X-Ray System Terminology

Manual X-ray Inspection (MXI) and Automated X-ray Inspection (AXI) - X-ray inspection systems are available in both manual (MXI) and automated (AXI) configurations. MXI systems can have varying degrees of automation which can include automatic BGA analysis, automatic image processing functions, automated manipulation and board handling. Another feature available with transmission target x-ray systems is Oblique Viewing at High Magnification (see 7.3.3.2).

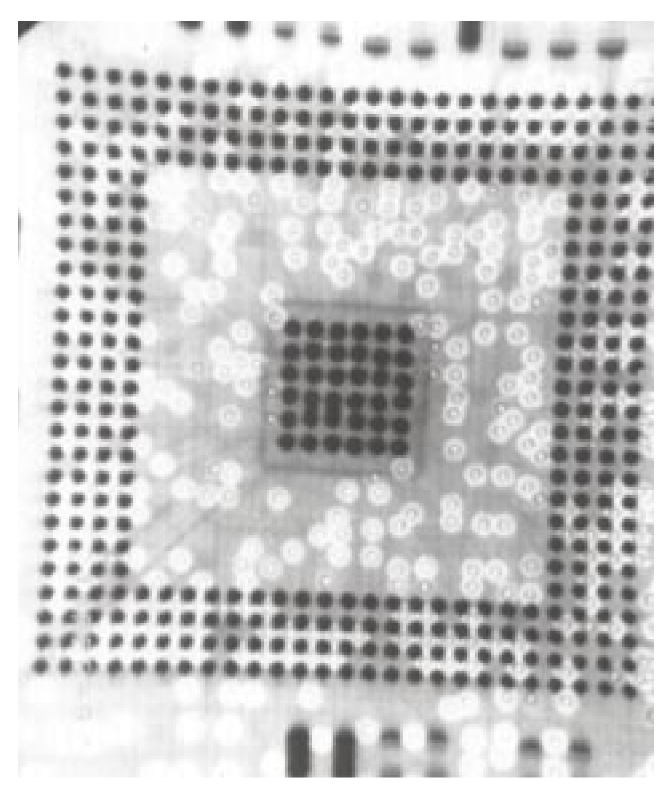


Figure 7-10 X-Ray Can Be Used to Detect BGA Package “Popcorning” (Pincushion Distortion)

What generally distinguishes AXI systems from MXI systems is that AXI systems are in-line capable and do not require an operator to make pass/fail decisions. MXI equipment is almost exclusively transmission X-ray technology whereas AXI equipment can be transmission, cross-section and combination.

AXI equipment is generally available in three forms:

- Transmission AXI - commonly referred to as ‘‘2D’’ X-ray
- Cross-Section AXI - commonly referred to as ‘‘3D’’ X-ray
- Combination 2D/3D AXI

The following definitions for Transmission, Cross-section and Combo Automatic X-ray Inspection apply:

Transmission x-ray automatically generates images of all features of the sample between the x-ray source and the detector. Figures 7-11 through 7-13 show examples of Transmission, Tomosynthesis, and Laminographic x-ray images.

Cross-section AXI automatically generates images of one slice of the board at a time. Laminography and tomosynthesis are the most common forms of cross-section AXI. Combo AXI equipment uses a combination of transmission and cross-section techniques concurrently during the inspection of a PCB. Combo systems automatically apply each technique where it is best suited and allow users the ability to prefer one technique to another if desired. On assemblies with components on both sides (Type 2), some subset of the solder joints will be inaccessible to the standard transmission x-ray technique due to overlap, unless an oblique viewing method is utilized.

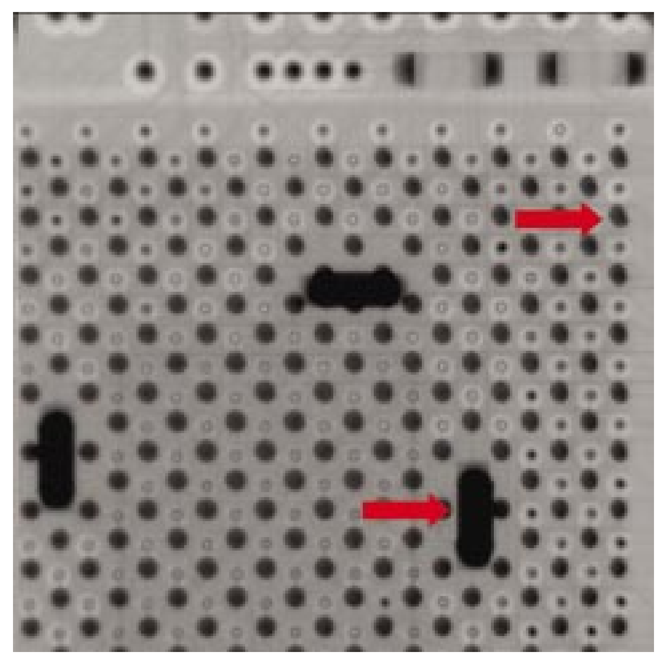


Figure 7-11 Transmission Image (2D)

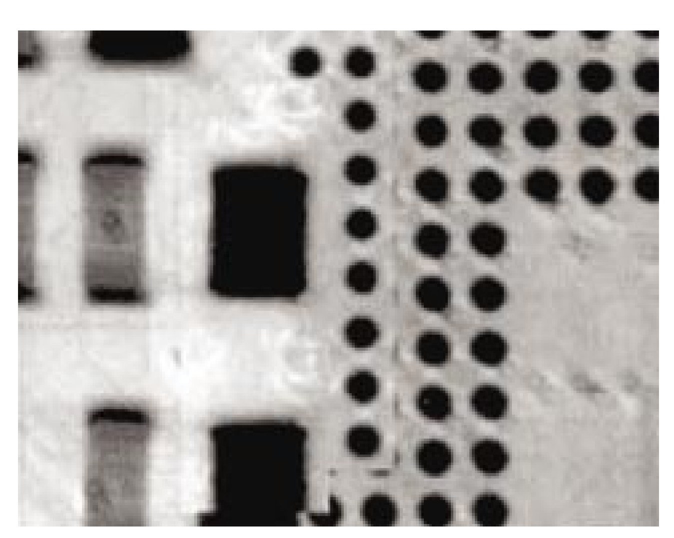


Figure 7-12 Tomosynthesis Image (3D)

The cross-section technique on the other hand, will have greater test access where oblique viewing is not utilized. Since the transmission x-ray technique captures information from the entire solder volume, and the cross-section technique captures specific ‘‘slice’’ information, these techniques have both unique & common capabilities to detect some types of solder defects. All of transmission, cross-section and combo x-ray techniques are capable of detecting PCB assembly defects that cause changes in the solder joint profile. These types of assembly defects include but are not limited to: solder shorts, solder opens, insufficient solder joints, missing devices, skewed devices, and solder voids.

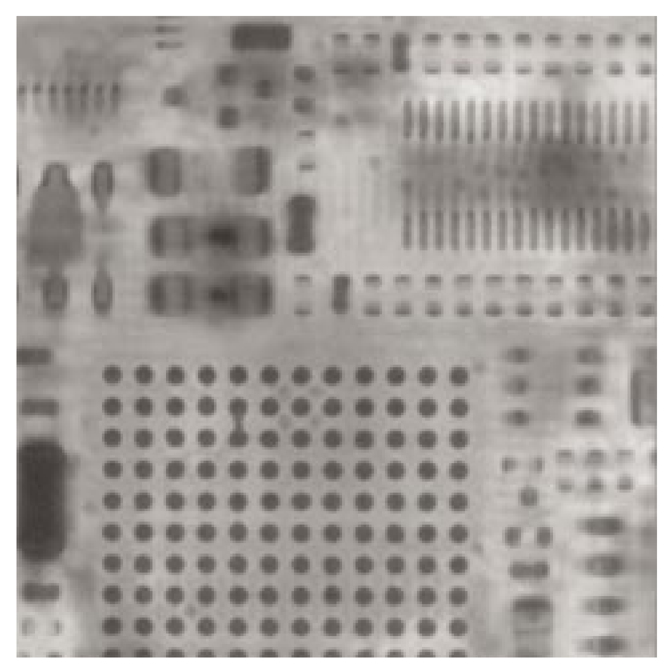


Figure 7-13 Laminographic Cross-Section Image (3D)

7.3.3.1 Transmission X-Ray Technology In transmission x-ray, the x-ray source and detector can be fixed or movable in a variety of motions for variations in magnification and angle of view. Generally, all features in the vertical ''line of sight'' are viewed concurrently without distinguishing depth.

Differences in material thickness or density will result in different transmitted x-ray attenuation at the detector resulting in brighter or darker intensities within the image display. For a single material type, such as eutectic solder, the attenuation of the x-ray photons received at the detector is proportional to the material thickness. A gray scale image is created which can be interpreted to determine whether or not solder joints are acceptable. Figure 7-14 shows a transmission inspection illustration.

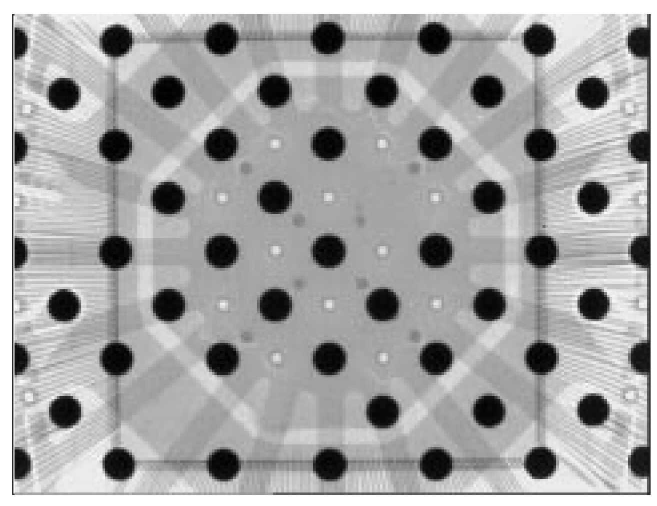


Figure 7-14 Transmission Example

7.3.3.2 Oblique Viewing Inspections with Transmission X-Ray Technology There are two basic methods of oblique viewing of objects with transmission x-ray systems. One method consists of tilting the sample in order to get the oblique angle as illustrated in Figure 7-15. Although this method enables the oblique view, the technique will not allow for the highest achievable level of magnification to be realized.

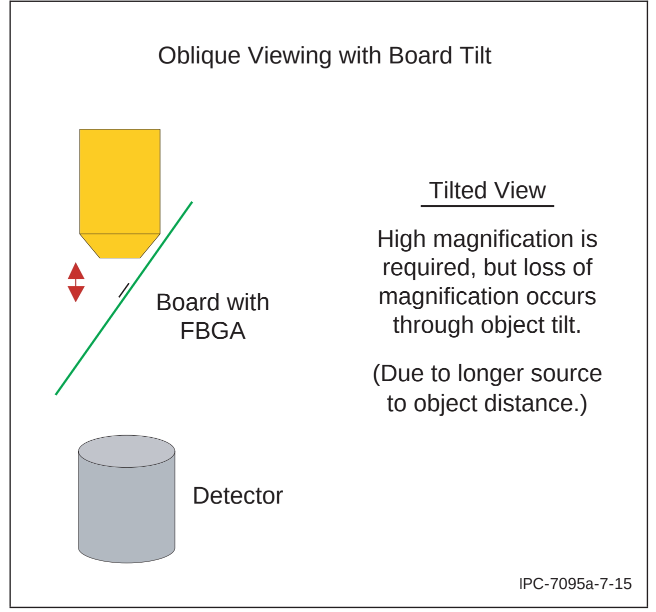


Figure 7-15 Oblique Viewing Board Tilt

Another method of oblique viewing utilizes a wide angle transmission x-ray source as illustrated in Figure 7-16. In this method, the detector rotates around the center axis of the x-ray source, utilizing the peripheral portion of the cone of radiation to produce an oblique view with the highest achievable magnification.

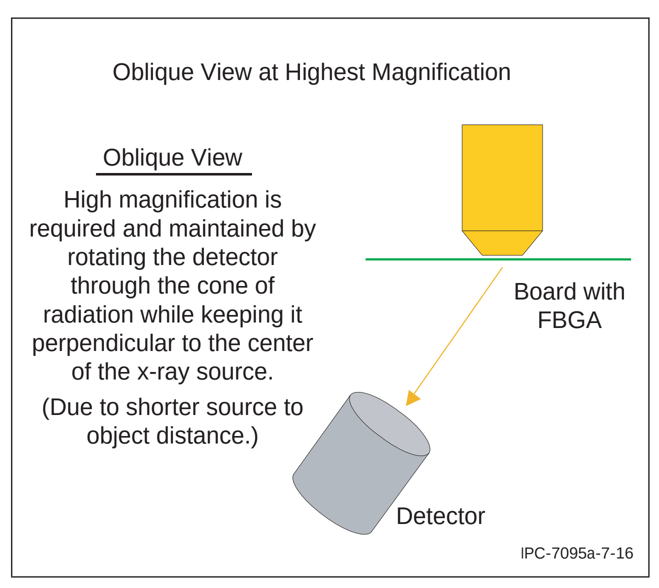


Figure 7-16 Oblique Viewing Detector Tilt

Figures 7-17 and 7-18 illustrate the benefits of oblique viewing at high magnification with actual images of a FBGA comparing a top down transmission view with an oblique view.

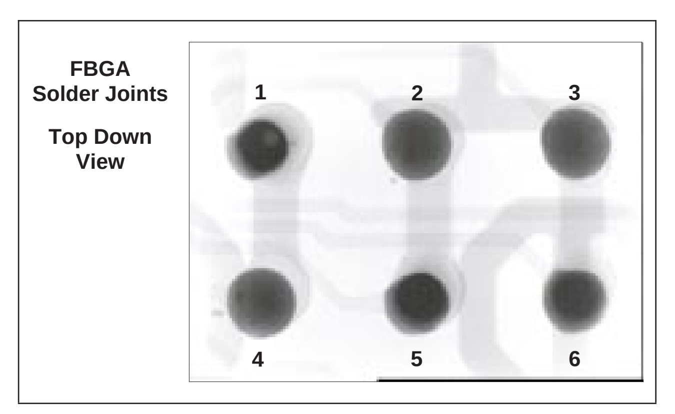
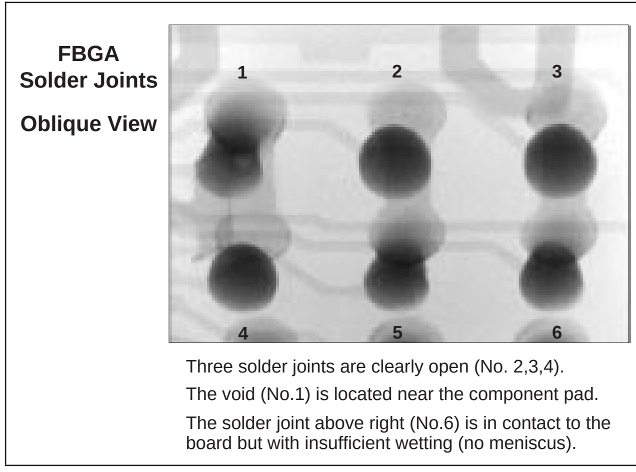


Figure 7-17 Top Down View of FBGA Solder Joints



Three solder joints are clearly open (No. 2,3,4).
The void (No.1) is located near the component pad.
The solder joint above right (No.6) is in contact to the board but with insufficient wetting (no meniscus).

Figure 7-18 Oblique View of FBGA Solder Joints

7.3.3.3 Cross-Sectional X-Ray Technologies On double sided boards, some subset of the solder joints will be inaccessible to the transmission x-ray technique due to overlap whereas the cross-section technique will have greater test access. Because the transmission x-ray technique captures information from the entire solder volume and the cross-section technique captures specific ''slice'' information, these techniques have both unique & common capabilities to detect some types of solder defects. For more detailed information, contact the manufacturers of AXI systems who can provide information about the capabilities of their techniques and systems.

Both tomosynthesis, Figure 7-19, and laminography, Figure 7-20, are radiographic techniques that provide image ''slices'' of the device can be viewed. With laminography, the x-ray source and the x-ray image plane are moved in a coordinated way with respect to the electronic device being inspected. A clear image of only one layer or ''slice'' of the device appears; all other layers in the image plane are blurred out. Tomosynthesis collects several transmission x-ray images from different angles during the inspection and combines the digital data of those images mathematically. This enables virtual slices to be created at the desired plane for analysis.

7.3.4 Analysis of the X-Ray Image An understanding of the construction of the particular BGA device and of the reflow process will aid in the interpretation and analysis of the x-ray image of the ball bonds. The concurrent factors that should be considered for x-ray image analysis might include:

1. Determine if the balls are collapsible (eutectic) or noncollapsible (noneutectic).
2. Define if noncollapsible balls have been placed in the corners to retain coplanarity.
3. Was reflow temperature maintained sufficiently to permit full alignment and collapse.
4. Does BGA package appear to have physically deformed in some way during reflow.

These factors will add further insight into the interpretation and analysis of the x-ray image.

7.3.4.1 Field of View In determining the criteria for inspections it is also important to determine how much can be seen of the BGA at any one time. As the pitch of the BGA gets smaller, the ball size is also reduced. Several magnification levels can be applied to the evaluation. Table 7-5 provides the different pitch and ball size characteristics applicable to any field of view. The magnification range varies, however should be between 30X and 50X. Depending on the ball size, the field of view can be determined by simply dividing the number ''15'' by the ball size. Thus, 15

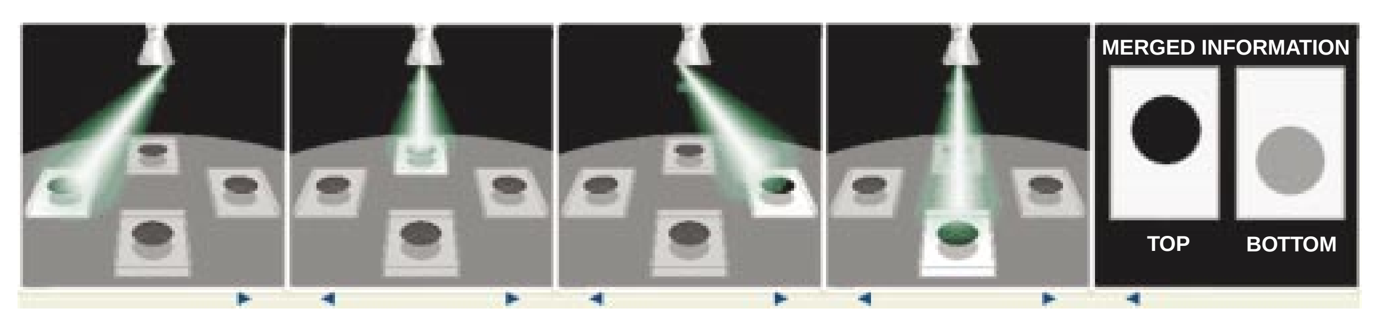


Figure 7-19 Tomosynthesis

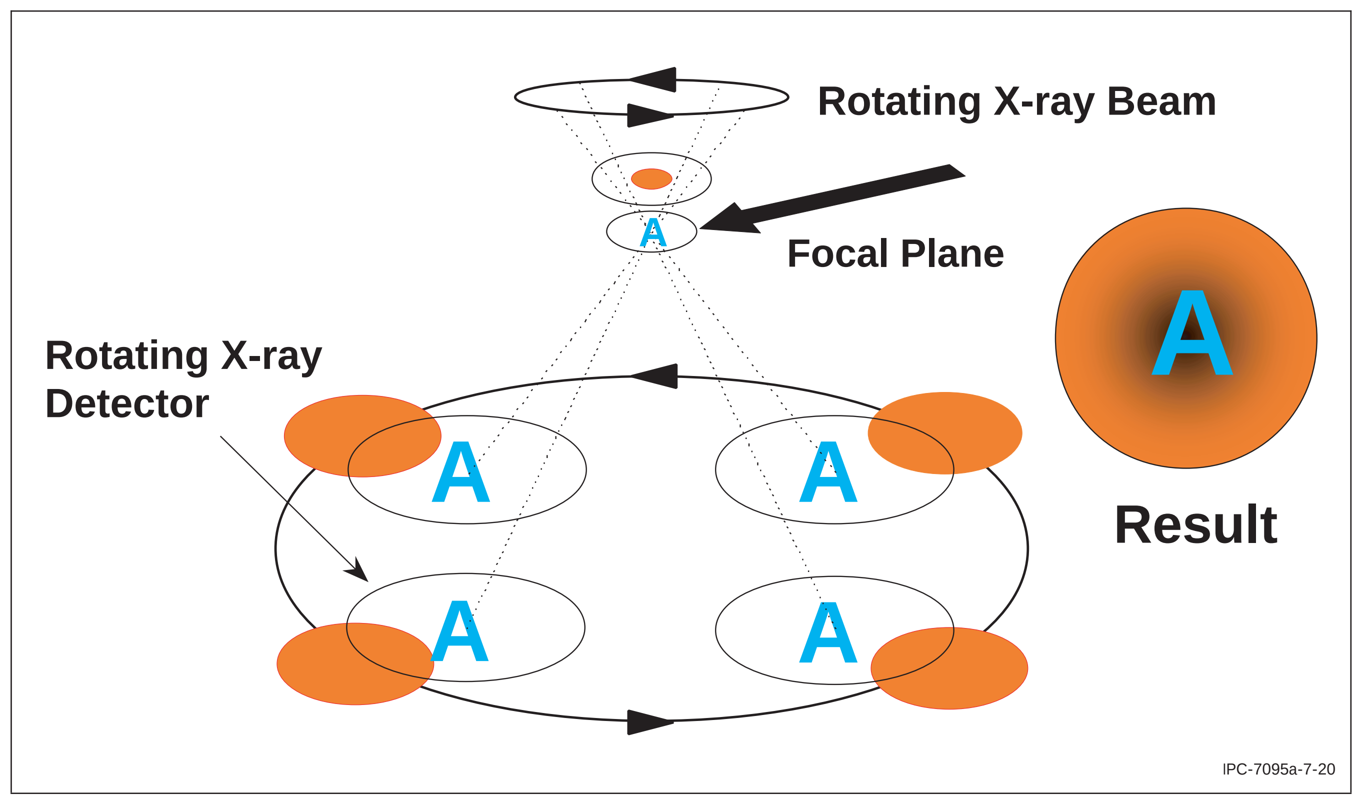


Figure 7-20 Scanned-Beam X-Ray Laminography

Table 7-5 Field of View for Inspection

Nominal Ball Diameter (mm)	Pitch (mm)	Magnification Recommendation	Field of View
0.75	1.5, 1.27	30X - 50X	15/0.75 = 20 Balls
0.60	1.0		15/0.60 = 25 Balls
0.50	1.0, 0.8		15/0.50 = 30 Balls
0.45	1.0, 0.8, 0.75		15/0.45 = 34 Balls
0.40	0.80, 0.75, 0.65		15/0.40 = 38 Balls
0.30	0.8, 0.75, 0.65, 0.50		15/0.30 = 50 Balls

divided by 0.75 (for the 0.75 mm ball) results in being able to see 20 balls of that size for evaluation. As the ball size decreases, a greater number of ball images are viewed for quality evaluations.

7.3.5 Scanning Acoustic Microscopy Scanning Acoustic Microscopy (SAM), also called Scanning Acoustic Tomography (SAT), is a nondestructive failure analysis tool. It uses sound waves to scan the internal layers of an assembly. It is commonly used in the semiconductor packaging field to detect delamination or voids located inside an electronic assembly. It can locate delamination or voids inside a BGA package. It can also locate similar anomalies in underfill after the BGA has been attached to the substrate.

The resolution of delamination or void detection depends on the acoustic frequency used for analysis. Resolution increases with increasing frequency. A 230 MHz transducer can bring detection resolution down to around a 25 µm gap.

A single point observation is called a SAM, a line scan is called a b-SAM, and an area scan is called a c-SAM. The c-SAM image in Figure 7-21 shows the location of voids in underfill in a flip chip assembly. The sample being inspected needs to be in water during the SAM analysis. Voids or delaminations that are open to water ingress cannot be detected with this method.

7.3.6 BGA Standoff Measurement Feeler gauges provide a nondestructive method of determining the approximate finished standoff of the BGA after reflow. Feeler gauges can be used at each corner after reflow and the combined results can be used to determine an average standoff measurement. This method is not as accurate as cross-sectioning but it is much less expensive and nondestructive. It does require adequate space around the BGA for the feeler gauges to be inserted. The standoff height of a BGA can give some indication that the solder balls reflowed completely and uniformly. The standoff of a typi-

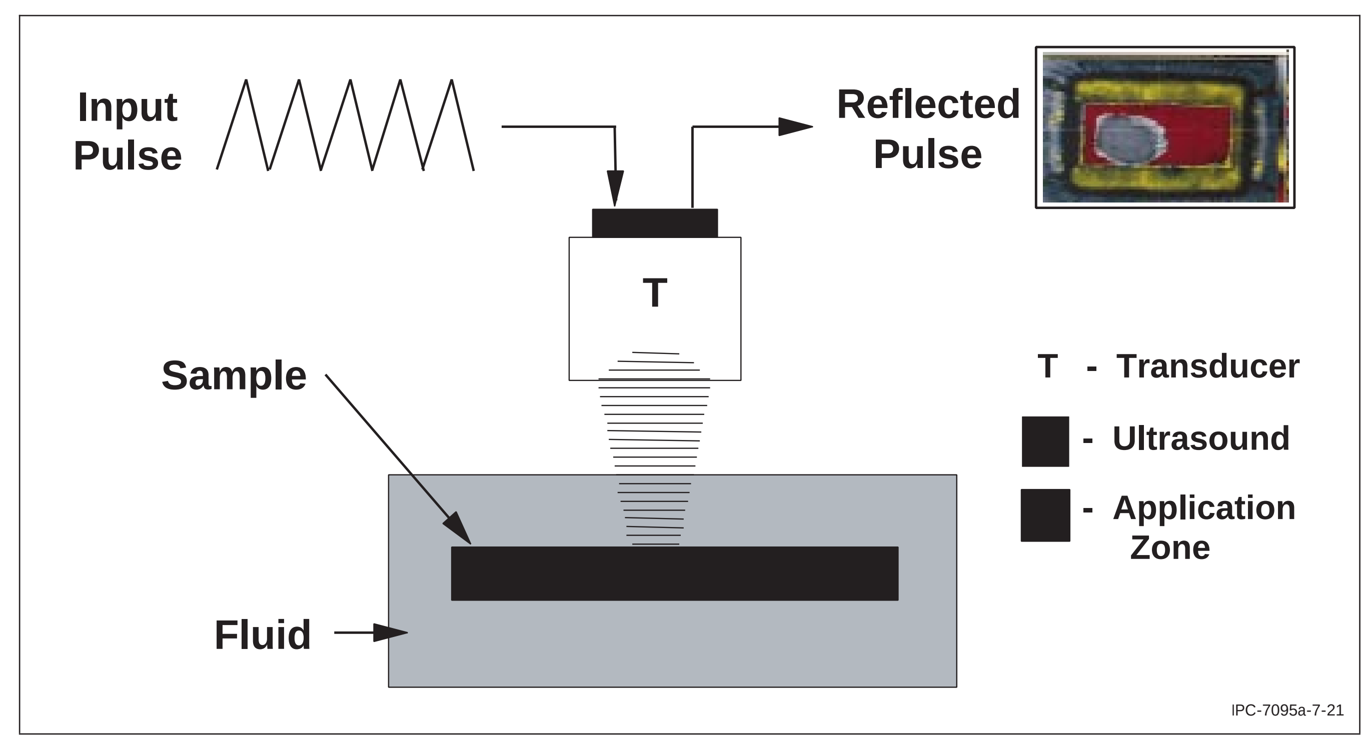


Figure 7-21 Scanning Acoustic Microscopy

cal PBGA with a 0.75 mm ball is approximately 0.60 mm prior to reflow and drops to 0.45 mm (including solder paste) after reflow.

7.3.7 Optical Inspection Endoscopy is an optical inspection method that permits visual inspection of tiny objects in a small, confined area. This technology has been adapted and applied to BGA solder joint inspection. BGA solder joints can be inspected and analyzed for a variety of critical factors such as:

- Overall Solder Joint Quality - evidence of proper wetting.
- Solder Joint Shape - evidence of proper reflow.
- Solder Joint Surface Texture - smooth vs. irregular.
- Overall Solder Joint Appearance - flux residue, etc.
- Solder Joint Defects - solder shorts, opens, cold solder.

This technology is best suited for inspecting exterior row BGA solder joints as shown in Figure 7-22. A limitation of this technology is the inability to view interior rows with the same level of quality and clarity. It is possible to focus on interior solder joints but not at the same level of detail as the exterior rows.

Lens design is a distinguishing feature of this technology. The highly advanced lenses are able to focus and redirect an image 90° using a mirror or prism. A high-resolution CCD camera and monitor are used to capture and display the image. Magnification, depending on working distance, ranges from 50x to 200x.

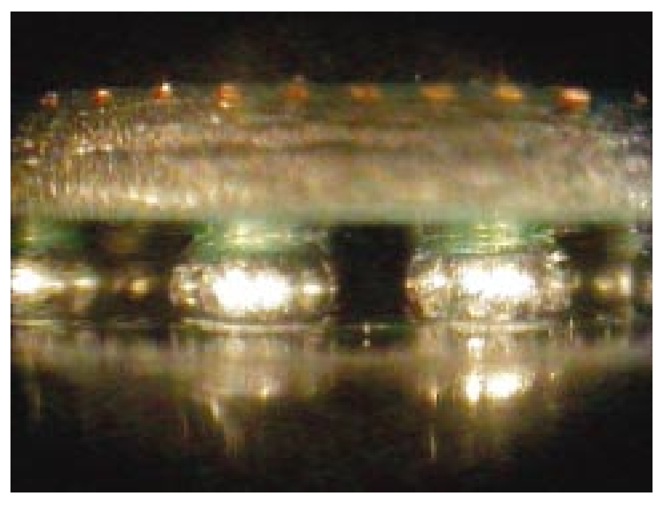


Figure 7-22 Endoscope Example

Lighting is a critical factor. The image quality will be poor if the light source does not properly illuminate the solder joint being inspected. Front lighting permits frontal inspection of a solder joint while back lighting is useful for detecting solder shorts and other obstructions. Back lighting also displays the solder joint outline which makes it easy to view the overall shape.

A robust positioning system that provides adequate support and protection for the lens and CCD camera is essential. It must eliminate motion due to shock and vibration and it must be adjustable through the desired range of motion.

Analytical software is also desirable. In addition to displaying a real time image of the solder joint it is useful to have

features such as image capture and measurement. Some systems provide reference photographs of acceptable and unacceptable solder joints. These images can be compared simultaneously with the image being evaluated, which reduces subjectivity during inspection.

In addition to simply viewing solder joints, this technique can be used to identify cracked peripheral interconnects (solder joints). Using a torque limited screwdriver an engineer can apply a small force which will separate fractured surfaces. This technique enables an engineer to determine, in a nondestructive manner, whether there is an open connection as shown in Figure 7-23. The engineer can also determine if the open is due to a lifted land, interfacial fracture or bulk solder failure. This technique does not work on some substrates, typically those of low thickness laminates which produce a more flexible component substrate (interposer).

7.3.8 Destructive Analysis Methods If the nondestructive measures used to identify a malfunction do not succeed in eliciting the cause of failure, then destructive analysis techniques may be used. Such techniques will render the analyzed assembly unusable. Once the cause of the failure has been identified the information can be used to implement corrective actions to eliminate the problem.

7.3.8.1 Cross-Sectioning If nondestructive methods fail to identify the cause of an anomaly, it may be necessary to use destructive methods to isolate the problem area. One-such method is cross-sectioning, which looks at a section of the components, substrate and solder joints after cutting it apart.

The first step in cross-sectioning is to identify or make a ''best guess'' regarding the area that needs to be examined. If more than one area is suspect then it needs to be determined whether those areas can be accessed sequentially on the same component. If not, then the areas will need to be prioritized according to the possibility of finding the problem or more than one component will need to be analyzed.

Next, if the problem area is a part of a larger assembly, it may need to be isolated into a small more manageable portion by cutting it out of the larger assembly. Care should be taken to ensure that the evidence is not tampered with or destroyed during the cutting process.

For proper sectioning, the sample should be molded in resin to alleviate chipping or destruction of the sample during cross-sectioning (see Figures 7-24 and 7-25). If fine

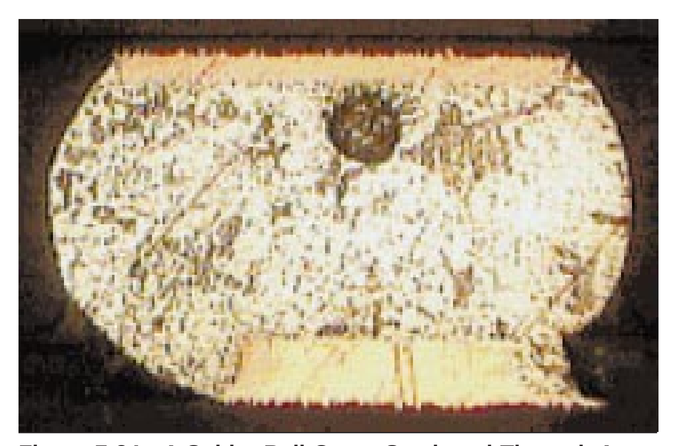


Figure 7-24 A Solder Ball Cross Sectioned Through A Void in the Solder Ball

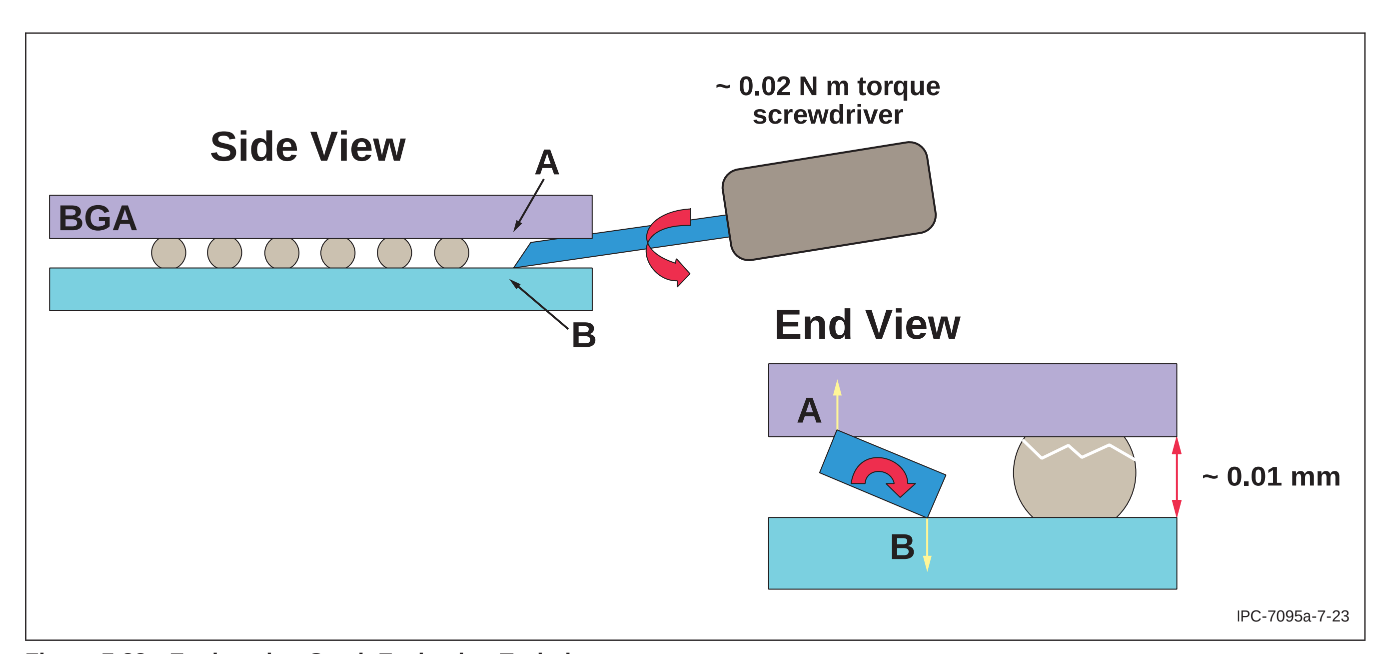


Figure 7-23 Engineering Crack Evaluation Technique

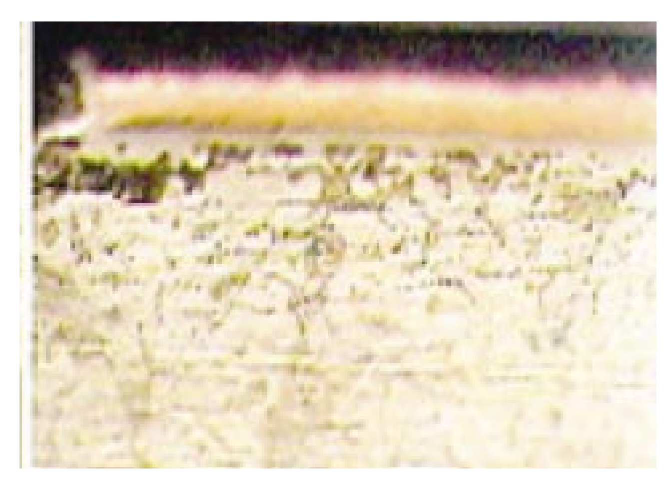


Figure 7-25 Cross-Section of a Crack Initiation at the Ball/Pad Interface

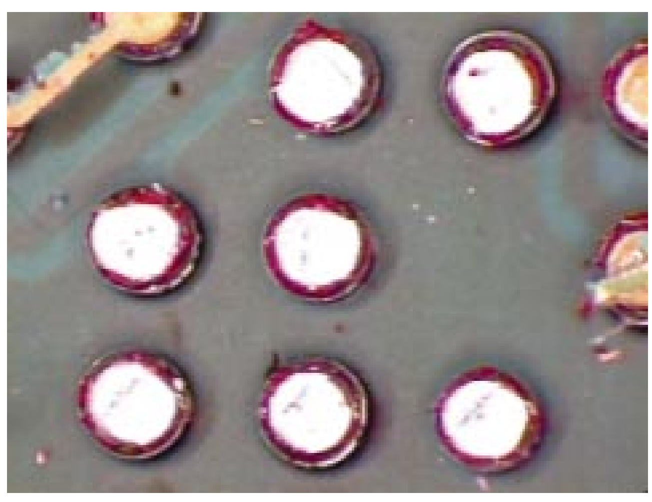


Figure 7-26 No Dye Penetration Under the Ball

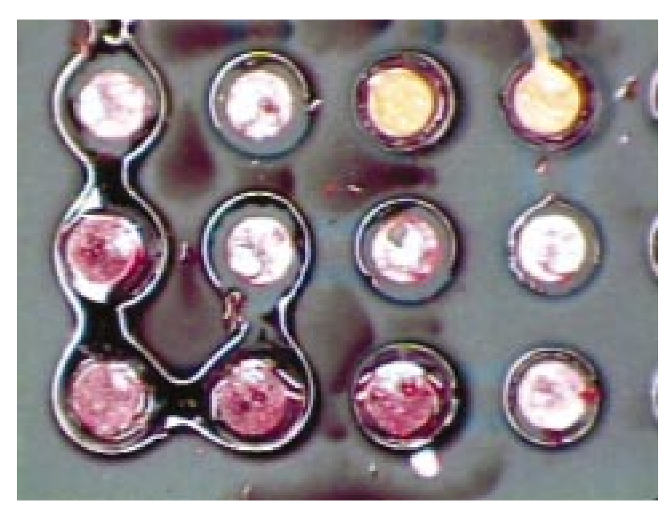


Figure 7-27 Corner Balls have 80-100% Dye Penetration which Indicate a Crack

polishing of the area of interest is going to be required then the sample should be sectioned a reasonable distance away from the interface of interest leaving sufficient distance for fine polishing of the interface.

In some cases, the entire component may need to be ground through and looked at for the integrity of various interfaces. A common failure analyzed through cross-sectioning is an open occurring in an assembly. Such opens may occur at the solder interface.

7.3.8.2 Dye Penetrant Dye penetrant methods can be used during process set-up and in failure analysis to detect solder joint cracking and wetting problems, and package delamination. The sample is immersed in a low viscosity liquid dye, which penetrates any cracks, delaminated areas, or open voids. The sample can then be peeled away and examined for the presence of dye in the solder joints or at material interfaces. If a fluorescent dye is used, the sample is inspected under UV light. The dye enhances the visibility of flaws that might otherwise be difficult to detect. Alternatively, the BGA can be mechanically pried off the board after dye penetration, and the solder lands examined. The presence of dye on a solder land indicates poor wetting to the land, and can be used to estimate the proportion of the land that was not wetted (see Figures 7-26 and 7-27).

7.4 Testing and Product Verification

7.4.1 Electrical Testing Electrical testing is used to evaluate the functionality of the electronic assembly. There are two commonly used electrical test approaches: In-circuit Test (ICT) and Functional Test (FT).

ICT utilizes a dedicated bed-of-nails fixture to probe the completed assembly. This test method is used to detect faults caused by the manufacturing process and also to isolate the majority of nonfunctional components. The fault spectrums for ICT includes solder bridge, solder open, component misorientation, wrong component, component not functional and conductor short.

Another approach is to place a low cost in-circuit tester near the end of the assembly line and use it as a manufacturing defect analyzer (MDA). Boards are tested immediately after the components are placed and soldered. Problems are quickly relayed back to manufacturing so corrective action can take place while the product is being assembled.

ICT can be supplemented by a complete functional test at the end of assembly. This test for product functionality can, depending on type of product and the acceptability requirements, be as simple as a ‘‘go/no-go’’ test or as complex as a complete exercising of all circuit functionality. FT is used to detect device faults on the assembly at speed.

7.4.2 Test Coverage Given the current complexity in electronic assemblies the level of ‘‘coverage’’ of test has become an industry issue. The more complex a board or assembly the more difficult it is to fully test. Indeed, it may be difficult to test even a reasonable portion of the assembly in a reasonable, i.e., cost effective, period of time.

While test of an assembly may be aided by incorporating test into the silicon devices this strategy is not applicable to bare boards. Thus the challenge of test is to provide test coverage at a high level of confidence within a reasonable period of time.

An effective process monitoring system consists of overlapping tools that create a large bandwidth of coverage. Multiple tools and methods are required since there is not one single tool or method that provides the desired coverage. Optical inspection, x-ray, SAM, ICT and FT are examples of overlapping coverage. These verification methods should be used to monitor products and process; they should not be used solely to screen and separate good and bad product.

7.4.3 Burn-In Testing Burn-in is an operational and environmental test of the complete assembly at the upper limits of the application. This test typically finds more component related problems than solder joint defects. The use of burn-in testing is still in use for component evaluation. Burn-in on electronic assembly is decreasing in favor of some form of accelerated test exposure to screen out marginal results.

7.4.4 Accelerated Reliability Testing The validation and qualification tests should follow the guidelines given in IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments and/or IPC-9701, Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments. For some products, the accelerated temperature cycling (ATC) needs to be combined with mechanical shock and/or vibration testing.

Accelerated reliability testing is carried out on design prototypes, typically to failure or until a predetermined reliability goal is achieved. The appropriate reliability goal can be determined with an appropriate acceleration model (see IPC-D-279, Design Guidelines for Reliable Surface Mount Technology Printed Board Assemblies).

Once failure occurs, the resulting failure modes are analyzed as to the underlying failure mechanism(s). If it fails expectations then corrective action is necessary. Either the assembly process needs to be improved or the product needs to be redesigned. In either case retesting may be necessary after the corrective action has been implemented.

Recognizing that a matrix was needed to determine the exact requirements and the testing necessary for performance performance under various conditions the IPC Product Reliability Committee developed the following table ''Product Categories and Use Environments.'' Table 7-6 attempts to relate seven product categories by typical application to the thermal, mechanical, atmospheric, and electrical performance requirements that they must meet during typical manufacturing processes, storage, and during operation.

7.4.5 Product Screening Tests Environmental stress screening (ESS) is used to screen ongoing production for poor product quality and latent defects. The purpose of ESS is to accelerate the latent defects to actual failures, thus eliminating these latent defects from causing failures in the field. Care must be taken that the ESS procedures are not sufficiently severe to damage good product and produce new latent defects.

7.5 Assembly Process Control Criteria for Plastic BGAs The greatest interest in BGA assembly acceptance is the degree of voids permitted in the attachment process and the impact on reliability. The detailed requirements for end product acceptance shall be in accordance with J-STD-001; workmanship requirements should follow the requirements of IPC-A-610.

This section establishes the practicable process development and maintenance criteria as well as attempting to address the issues related to an acceptable assembly process. The majority of the recommendations are based on the use of plastic BGAs with the eutectic solder balls as the Input/Output termination.

7.5.1 Voids Current industry data suggests that voids in the solder joint is not a reliability concern. However, a change in void size or frequency of voids may be an indication that the manufacturing parameters need to be adjusted. Two reported causes of voids are trapped flux that has not had enough time to be released from the solder paste, and contaminants on improperly cleaned circuit boards. Voids appear as a lighter area inside the solder balls and are usually found randomly throughout the package. X-ray systems tend to distort the size of voids due to blooming. It is possible to accurately measure the true volume of a void but the procedure can be involved and requires a known reference for radiometric calibration of the x-ray film or detector. In most cases the effort is better spent on identifying and eliminating the cause of the voids.

7.5.1.1 Sources of Voids There can be voids in a BGA solder ball, in the solder joint to BGA interface, or in the solder joint to PCB interface. Various sources or reasons can be responsible for these voids.

Voids can be carried over from original voids in solder balls, which could be the result of the ball manufacturing process. Voids can be induced into the reflowed solder joint by either the voids in the original component solder ball, or during the reflow attachment process. Voids can also form near the PCB to ball interface during BGA to PCB attachment. These voids are typically formed during the reflow soldering process by flux volatiles trapped during the solidification of the molten solder. The source of flux volatiles can be either from applied flux itself (typically rework), or flux which is one of the constituents of the solder paste used in the reflow assembly process.

Table 7-6 Accelerated Testing for End Use Environments

Worst-Case Use Environment								Accelerated Testing			
Use Category	**Tmin °C**	**Tmax °C**	**ΔT[1] °C**	**t_D hrs**	**Cycles/ Year**	**Typical Years of Service**	**Approx. Accept. Failure Risk %**	**Tmin °C**	**Tmax °C**	**ΔT[2] °C**	**t_D min**
1) Consumer	0	+60	35	12	365	1-3	1	+25	+100	75	15
2) Computers	+15	+60	20	2	1460	5	0,1	+25	+100	75	15
3) Telecom	-40	+85	35	12	365	7-20	0,01	0	+100	100	15
4) Commercial Aircraft	-55	+95	20	12	365	20	0,001	0	+100	100	15
5) Industrial & Automotive Passenger Compartment	-55	+95	20 &40 &60 &80	12 12 12 12	185 100 60 20	10	0,1	0	+100	100 & COLD[3]	15
6) Military Ground & Ship	-55	+95	40 &60	12 12	100 265	10	0,1	0	+100	100 & COLD[3]	15
7) Space leo geo	-55	+95	3 to 100	1 12	8760 365	5-30	0,001	0	+100	100 & COLD[3]	15
8) Military Avionics a b c	-55	+95	40 60 80 &20	2 2 2 1	365 365 365 365	10	0,01	0	+100	100 & COLD[3]	15
9) Automotive Under Hood	-55	+125	60 &100 &140	1 1 2	1000 300 40	5	0,1	0	+100	100 & COLD[3] & LARGE ΔT[4]	15

& = in addition

1) ΔT represents the maximum temperature swing but does not include power dissipation effects; for power dissipation calculate ΔT; power dissipation can make pure temperature cycling accelerated testing significantly inaccurate. It should be noted that the cyclic temperature range, ΔT is not the difference between the possible minimum, T_{min} and maximum, T_{max}, operational temperature extremes; ΔT is typically significantly less.

2) All accelerated test cycles shall have temperature ramps, 20°C/minute and dwell times at temperature extremes shall be 15 minutes measured on the test boards. This will give ~24 test cycles/day.

3) The failure/damage mechanism for solder changes at lower temperature; for assemblies seeing significant cold environment operations, additional ''COLD'' cycling, from perhaps -40 to 0°C, with dwell times long enough for temperature equilibration and for a number of cycles equal to the ''COLD'' °C operational cycles in actual use is recommended.

4) The failure/damage mechanism for solder is different for large cyclic temperature swings traversing the stress-to-strain -20 to +20°C transition region; for assemblies seeing such cycles in operation, additional appropriate ''LARGE ΔT'' testing with cycles similar in nature and number to actual use is recommended.

In addition to voids formed from via-in-pad construction (see 6.3.1), some voids are detected in the middle to top (ball/ BGA interface) of the reflowed solder joint. This is expected because the trapped air bubble and the vaporized flux, which is applied to the PCB BGA lands, rises during the reflow profile. This occurs when the applied solder paste and the BGA's collapsible eutectic solder ball(s) melt together during the reflow profile (typically 210 to 230°C peak temperature). If the reflow profile cycle doesn't allow sufficient time for either the trapped air or vaporized flux to escape, a void is formed as the molten solder solidifies in the cool down area of the reflow profile. Therefore, the development of the reflow profile is extremely important as a contributor to the formation of voids.

Voids in solder joints are not new; collapsible BGAs also share this characteristic. Voids can be detected under leaded components when using x-ray equipment. However leaded component solder joints were historically visually inspected, not x-rayed, and therefore never detected. The metallurgical composition and surface roughness of an incoming component ball can also add to ball void creation. BGA suppliers should x-ray components before and after the J-STD-002 Surface Mount Simulation Test (Test S) is run to reveal anomalies that may lead to solderability problems.

Voiding can be a result of surface contamination at the component land or PCB land, intermetallics forming

between solder ball and land, or un-expelled flux residues from the assembly process as shown in Figure 7-28.

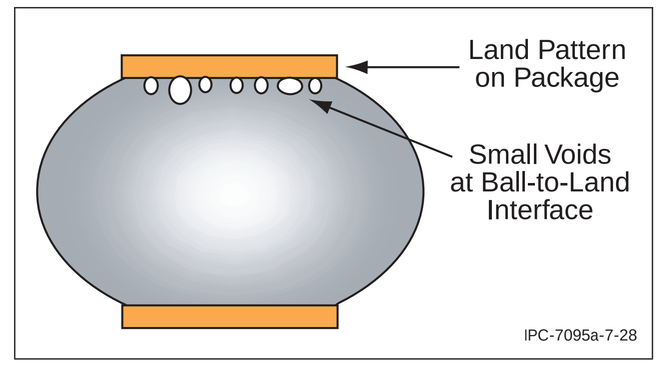


Figure 7-28 Small Voids Clustered in Mass at the Ball-to-Land Interface

7.5.1.2 Impact of Voids How many and what size of voids should be allowable in the product before they impact the product's required reliability? Voids may impact reliability by weakening the solder balls and reducing functionality because the reduced cross-section will have lower heat transfer and current carrying capabilities.

Large voids are more detrimental but small pre-existing voids can merge during reflow to create large voids. The elimination of voids, or at least a substantial reduction, is generally preferred.

There are a number of studies that have shown that a small increase in reliability is observed as a result of moderate size voids. These are typically from processes that are incontrol. The increased reliability results from increased solder joint height and a temporary and local retardation of crack propagation.

X-ray is required for the detection of voids in BGA solder joints; cross-sectioning may be necessary in order to determine the impact of the void or its location.

Low cost equipment is based on transmission x-ray. Unlike a leaded component, BGAs have solder joints that are not only on the component's periphery, but have internal solder joints that are not inspectable by normal visual techniques. Higher cost equipment is based on x-ray tomography or laminography. Both types of these systems provide valuable techniques for void detection and location. (see 7.3.1). It is recommended that the process be qualified for void acceptance before being released for production.

7.5.1.3 X-Ray Detection and Measurement Cautions Many of the real time x-ray inspection systems in use for the detection of solder voids employ an x-ray imaging device that exhibits an aberration referred to in the literature as ''Voltage Blooming'' or ''Phosphor Blooming.'' The manifestation of this aberration, shown in the accompanying images, (see Figure 7-29) is that light areas contained in a dark background (such as the appearance of a solder void) will grow or shrink in size as the voltage adjustment to the x-ray source is increased or decreased respectively. This change can be fairly large. The consequence is that the measurement of the actual size of the void becomes indeterminate. If it is determined that the x-ray inspection system in use exhibits voltage blooming, the following recommendations are made to obtain a more precise measurement of void size:

1. X-ray film images, not being subject to voltage blooming, have been found to provide a more accurate determination of void size. (Figure 7-30 is an x-ray image of a BGA void imaged on film, demonstrating the tonal accuracy of the film by revealing both the void and the die wire through the void.)

2. Correlation of the x-ray source voltage, to the degree of blooming, when the actual size of a void has been determined by cross sectioning or simulation. Note: The

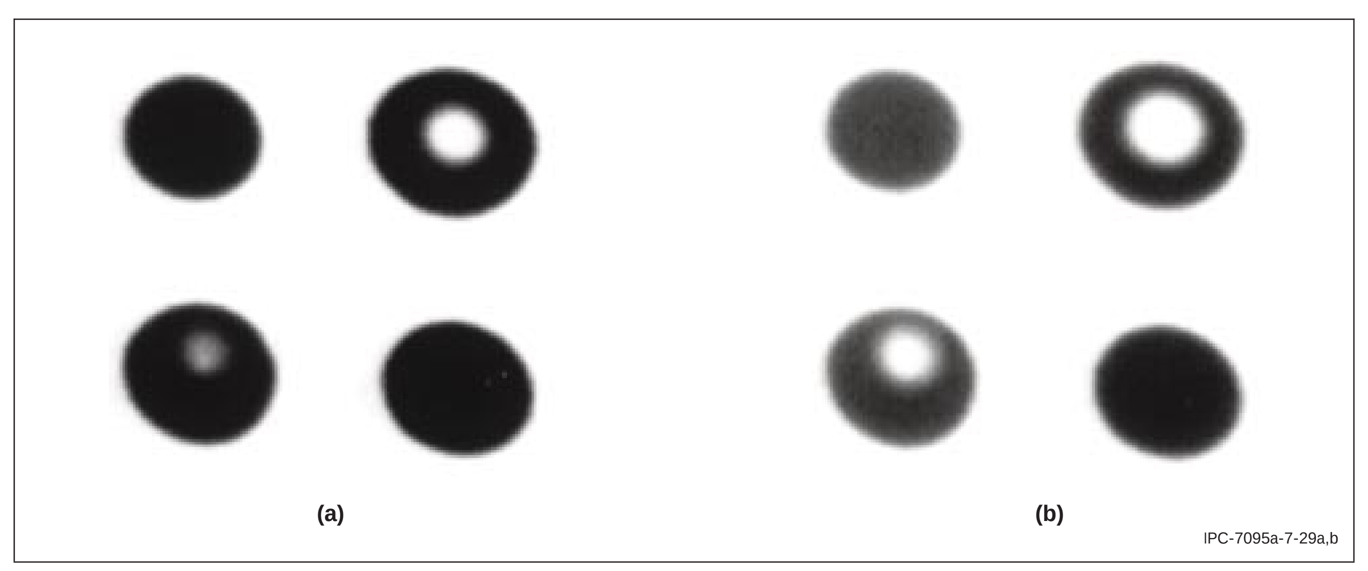


Figure 7-29 X-Ray Image of Solder Balls with Voids at 50 kV (a) and 60 kV (b)

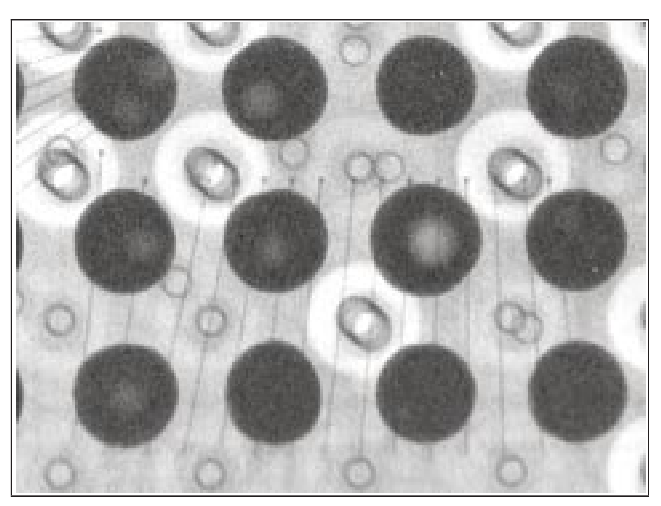


Figure 7-30 X-Ray Film Image of Voids

tonal quality should be good enough to see a wire through the void.

3. For every voltage and current setting, the gray scale should be reset to between 120 and 140, for a 1 to 256 gray scale system. Normalizing gray scale will maintain consistency between measurements.

7.5.1.4 Void Classification In order to assess different conditions, voids have been given a specific identifier, based on location, to establish a method of void identification and the possibility of corrective action for process improvement. The details are provided in Table 7-7 which shows a classification criteria for the location of voids in the BGA solder ball structure.

The following descriptions identify the five different void types:

Type A: Void(s) within the ball (package level) as received.

Type B: Void(s) at the ball/package substrate interface as received.

Type C: Void(s) within the ball after board level assembly process.

Type D: Void(s) at the ball/package substrate interface after board level assembly process.

Type E: Void(s) at the ball/board substrate interface after board level assembly process.

7.5.1.5 Control of Voids End users should work with their suppliers to control the frequency and size of voids in the BGA solder balls to some acceptable level. The suppliers can adjust their process and/or materials control in order to meet these objectives. Typically, few voids are detected in the incoming BGA solder joints.

Reflow time-temperature profile, flux amount, type and properties should be investigated for improvement. The formation of voids can also be influenced through material and/or process adjustment and optimization.

The use of excessive flux in the initial BGA attachment or in BGA rework has a tendency to create voids due to flux-volatilization. The process should be characterized to keep flux application to a minimum.

7.5.1.6 Process Control Criteria for Voids in Solder Balls There is a continuing need for process development and control to accommodate changing technologies. As BGA land sizes, solder ball sizes and land pitch continue to decrease, the dimensional parameters used on the production floor need to change. New materials and processes may be required to meet quality and reliability goals.

Voids will likely be encountered during various stages of product life from development through manufacturing. Maintaining a minimum acceptable standard is necessary to assure that the product meets customer expectations, product-life and reliability requirements. Manufacturers need to use process control and continuous product improvement techniques for void control. Readily available statistical process control and process improvement tools may be used.

Table 7-7 Void Classification

Void Analysis	Voids Within the Ball	Voids at the Package Interface	Voids at the Mounting Surface Interface
Voids in BGA balls prior to attachment to a PWB	Type A	Type B	N/A
Voids in BGA balls after attachment to a PWB	Type C	Type D	Type E

A change in frequency and size of voids should indicate a need for process control as well as improving the process and materials. A baseline can be used to determine the need for process adjustments to control the frequency and size of voids. As an example an acceptable limit goal could be established that no more than 5% of the solder balls have voids. In addition, a void size limit could be established. Size is determined in relationship to the ball. Thus a void size larger than 25% of the solder ball's cross sectional diameter is approximately 6% of the total contact area (see Figure 7-31). Any such process control limits should be set with customer agreed-to contractual commitment.

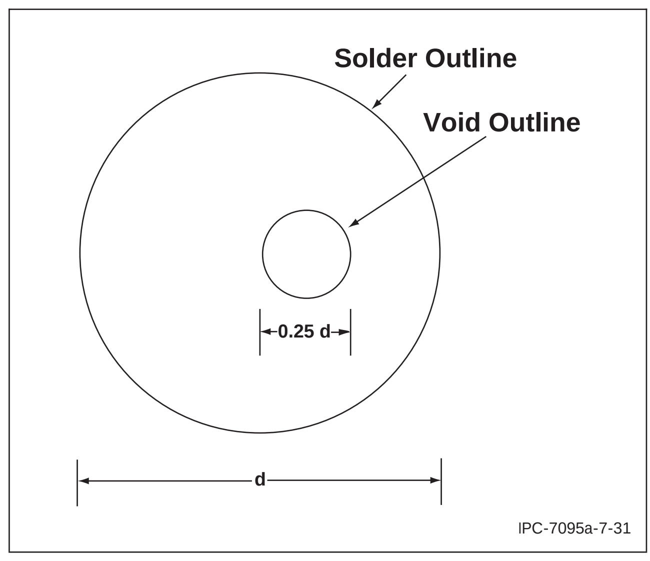


Figure 7-31 Example of Voided Area at Land and Board Interface

When there is more than one void per solder ball, the dimensions of the voids will be added to calculate the total voiding in that solder ball.

In regard to voids and the percentage of voids within the ball, location of the voids is of greater concern. There is no evidence or empirical data that indicates that voids within the ball will cause failure. Voids at the interface between the ball-and-package substrate as well as voids at the interface between ball-and-PCB will be more likely to contribute to solder joint cracking. This is because cracks (if they occur) will typically occur at the interface and the void or voids can provide (in time) a path to accelerate the cracking condition.

The determination of the impact that voids have on the final product can best be expressed in terms of the flow diagram shown in Figure 7-32.

7.5.1.7 Accept/Reject Criteria The accept/reject criteria for BGA assemblies is being considered by the J-STD-001 and IPC-A-610 Task Groups at the time of release of this standard. Those documents provide the final accept/reject criteria used in contractual agreements. The recommended accept/reject conditions have been supplied to those standard groups for consideration. The details are based on the experiences of the members of the IPC-7095 task group.

Void clarification is defined as to whether the voids occur prior to attachment to the mounting structure, or after the assembly has taken place. This useful information can be correlated to reliability conditions based on the end use environment. Using the size limitation structure a process can be established that helps to meet the customers' defined acceptability conditions.

Table 7-8 helps to validate process control conditions. The information is based on void size and follows the recommendations of the flow diagram shown in Figure 7-32. The combination of void location and void size helps to establish the acceptance levels in the standard IPC three class structure.

7.5.1.8 Process Characterization Table 7-9 identifies the particular void types and relates this information to the number of occurrences that there could be in the three performance classes adopted by IPC. The evaluation of an increase in the number of voids that has been set as a target value can be a good aide to determining a process shift or a required change in some of the process parameters.

A process change should be driven by an appropriate SPC methodology which should be used during normal production cycles. The use of Table 7-9 should also be used for new product introduction, product and process qualifications, equipment set changes, component qualifications, response to customer feedback, and any similar change to the process or parameters.

The sampling plan used should be done at a printed circuit assembly level, unless the SPC results show a component-related issue (for example, voids in one collapsible BGA and no voids across the other collapsible BGAs on the board). In this case, the sampling plan should be executed at a component level of the suspect component part rather than examining the assembly process.

7.5.1.9 Detectable Void Percentages With Respect to Different Solder Joint Diameters Considering a 0.20 mm diameter void as an example, Table 7-10 lists the void percentages for different ball sizes. The percentage void diameter detectable becomes larger as solder joint size decreases, that is, 27% on 0.75 mm joint inflates to 67% on 0.30 mm solder joint size.

Defective determination is made by the product's reliability requirements. As an example, if the maximum allowable void size is 30% of the solder ball diameter (equivalent to 11% of area). This can be either one void, or the summation of many voids. Some of the newer x-ray equipment use algorithms that are able to summarize the void areas. Unfortunately the current algorithms for x-ray tomography do not perform the summation of the voids.

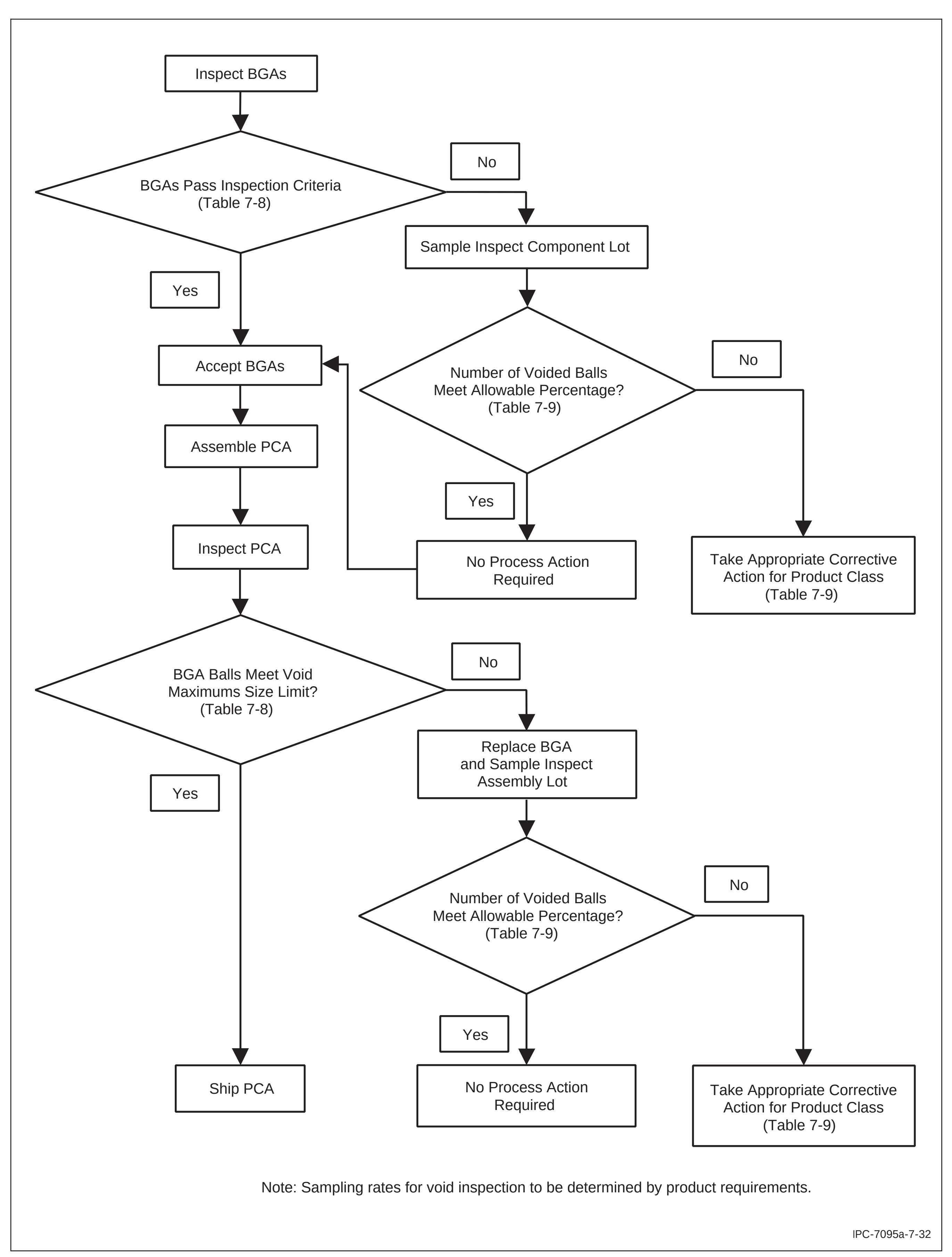


Figure 7-32 Typical Flow Diagram for Void Assessment

Table 7-8 Void Size Limitations

Void Type	Void Description	Process Control Criteria			Determined By
		Class 1	Class 2	Class 3	
A	Voids within the solder ball at incoming	36% of area = 60% of dia	20% of area = 45% of dia	9% of area = 30% of dia	Transmission or cross section X-ray (sampling)
B	Voids at Package Interface at incoming	25% of area = 50% of Dia.	12% of area = 35% of Dia.	4% of area = 20% of Dia.	Transmission * or Cross section X-ray (sampling)
C	Voids within the Ball after PCA reflow	36% of area = 60% of dia	20% of area = 45% of dia	9% of area = 30% of dia	Transmission * or cross section X-ray (sampling)
D	Voids at the package interface after PCA reflow	25% of area = 50% of Dia.	12% of area = 35% of Dia.	4% of area = 20% of Dia.	Transmission * or Cross section X-ray (sampling)
E	Voids at the mounting surface/ Printed Board after PCA reflow	25% of area = 50% of Dia.	12% of area = 35% of Dia.	4% of area = 20% of Dia.	Transmission * or Cross section X-ray (sampling)

If Transmission X-ray is used to evaluate the occurrence of voids the tightest criteria (% allowable at ball or interface) must be used for the evaluation since transmission X-ray cannot determine the location of the void. This would be the criteria for a type ''D'' void.

Table 7-9 Corrective Action Indicator

Void Type	Void Description	Corrective Action Indicator			Action Taken
		Class 1	Class 2	Class 3	
Determined by cross section/X-ray laminography (sampling according to Section 7.5.1.10)					
A	Voids within the solder ball (prior to assembly)	>20% balls have voids	>10% balls have voids	>5% balls have voids	Investigate root cause in process & take corrective action.
B	Voids at package interface (prior to assembly)	>10% balls have voids	>8% balls have voids	>3% balls have voids	Investigate root cause in process & take corrective action.
C	Voids within the ball after PCA reflow	>30% balls have voids	>20% balls have voids	>10% balls have voids	Investigate root cause in process & incoming parts, take corrective action.
D	Voids at the package interface after PCA reflow	>10% balls have voids	>8% balls have voids	>3% balls have voids	Investigate root cause in process & incoming parts, take corrective action.
E	Voids at the mounting surface interface after PCA reflow	>15% balls have voids	>10% balls have voids	>5% balls have voids	Investigate root cause in process & incoming parts, take corrective action.
Determined by transmission X-ray (sampling according to Section 7.5.1.10)					
A, B	Voids at incoming	>10% balls have voids	>8% balls have voids	>3% balls have voids	Investigate root cause in process & take corrective action.
C, D, E	Voids after PCA reflow	>10% balls have voids	>8% balls have voids	>3% balls have voids	Investigate root cause in process & incoming parts, take corrective action.

Note 1: Ball with cumulative voids smaller than 15% diameter (2% by area) are not counted.
Note 2: These limits do not apply to uncapped via-in-pad solder joints.

Table 7-10 Ball-to-Void Size Image - Comparison for Various Ball Diameters

Solder Ball Diameter/ X-Ray Image	Void 0.20 mm Diameter	
	% Void Diameter	% Void Area
0.85 mm	24%	6%
0.75 mm	27%	7%
0.65 mm	31%	9%
0.55 mm	36%	13%
0.45 mm	44%	20%
0.40 mm	50%	25%
0.30 mm	67%	44%

For a single void, X-ray tomography can identify a defect caused by a void that is greater than the pre-determined size.

Example: If the solder ball size = 0.75 mm and the maximum allowable void size = 30% of the ball diameter, the maximum void size at the center of the ball would be calculated as follows.

30% of 0.75 mm

(0.75 mm)(0.3) = 0.225 mm maximum void diameter

When the void is not in the center of the ball and near the land of either the board or the component, the cross sectional diameter of the ball will be reduced as well as the maximum allowable size for a void.

Example: If the ball diameter at the land is approximately equal to the land and the land size is 75% of the ball size (25% reduction) then:

75% of 0.75 mm = 0.56 mm ball diameter at the land
30% of 0.56 mm = maximum void diameter
(0.56)(0.3) = 0.17 mm maximum void diameter at the land.

Process control criteria for the number and size of voids discourages a general presence of voids which indicates an

out of control process and indicates the need to use the necessary tools for process and material improvement. Void size is also important as shown in Table 7-8 and Figure 7-33. The criteria defines the characteristics for void acceptability based on size.

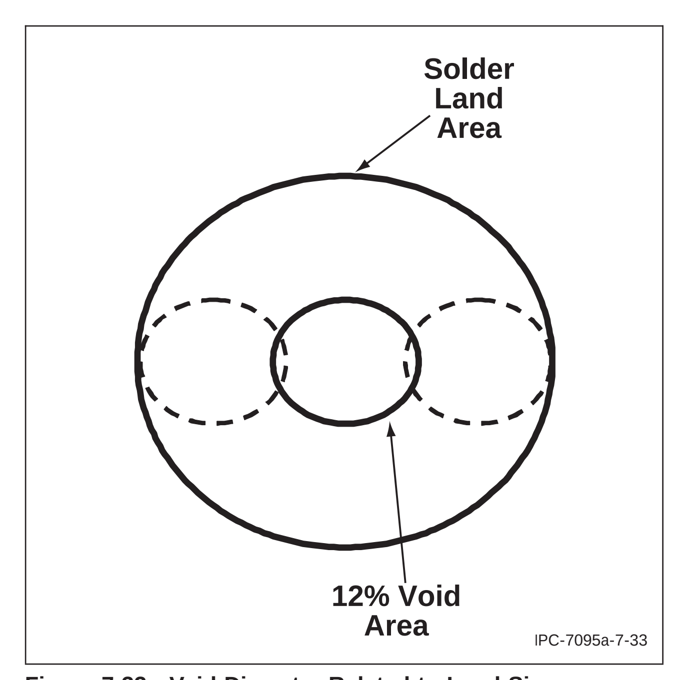


Figure 7-33 Void Diameter Related to Land Size

[1] Note: By prior agreement between supplier and customer, the maximum void area may be greater or less than the dimensions shown in Table 7-8.

For the collapsible solder balls, when attached to the land pattern, the ball takes an elliptical sphere form rather than a uniform round sphere shape. Therefore, the solder joint diameter at the balls center is typically greater than the diameter at the ball-to-land interface. The criteria applied to varying ball sizes and land sizes will result in different void sizes.

7.5.1.10 Sampling Plans for Void Evaluation Because of the industry concern regarding voids, this standard attempts to define criteria for void baseline goals and process control techniques. Everyone agrees that it makes no sense to throw away good product, or rework product where a void is identified without some indication as to the complexity and the impact on reliability of that condition.

Void occurrence criteria are not based on 100% inspection, but are accomplished through the use of sampling plans. The sampling plan conditions are identical to those shown in IPC-6012 and are repeated in Table 7-11. It should be noted that the table is based on C=0. What this means is that, as within all IPC standards, when a sample is selected, any occurrence of exceeding the characteristics for void size shown in Table 7-8, requires 100% evaluation of the total lot.

The appropriate corrective action may vary based on class of product and customer requirements. The ultimate action is to remove and replace the affected component, however those solutions must be carefully evaluated as the product should have been designed to permit repair procedures that include reevaluation.

7.5.2 Solder Bridging Solder bridging is unacceptable. Electrical testing, optical inspection or x-ray inspection is necessary to detect solder bridging. Poor solder paste printing, inaccurate placement, manual ''tweaking'' after placement, and solder splattering during reflow are typical causes of solder bridging. Solder balls too large for the gap between the two substrates can also cause bridging.

Table 7-11 C=0 Sampling Plan (Sample Size for Specific Index Value*)

Lot Size	Class 1			Class 2			Class 3			
	2.5*	4.0*	6.5*	1.5*	2.5*	4.0*	0.10*	1.0*	2.5*	4.0*
1-8	5	3	2	**	5	3	**	**	5	3
9-15	5	3	2	8	5	3	**	13	5	3
16-25	5	3	3	8	5	3	**	13	5	3
26-50	5	5	5	8	5	5	**	13	5	5
51-90	7	6	5	8	7	6	**	13	7	6
91-150	11	7	6	12	11	7	125	13	11	7
151-280	13	10	7	19	13	10	125	20	13	10
281-500	16	11	9	21	16	11	125	29	16	11
501-1200	19	15	11	27	19	15	125	34	19	15
1201-3200	23	18	13	35	23	18	125	42	23	18
3201-10,000	29	22	15	38	29	22	192	50	29	22
10,001-35,000	35	29	15	46	35	29	294	60	35	29

*Index Value is associated to the A.Q.L. value. If a particular product is determined to be ''critical'' by the user and a smaller index value is required, the user **shall** designate the requirement in the procurement document and should state the ''critical'' requirement on the master drawing.
**Denotes inspect entire lot.

7.5.3 Opens Solder opens are also unacceptable. Electrical testing, optical inspection or x-ray inspection is necessary to detect solder opens. Poor solder paste printing, inaccurate placement and manual ''tweaking'' after placement are typical assembly related causes of solder opens. Coplanarity and substrate solderability problems can also cause opens. Excessive mechanical stress can also cause solder joints to crack and create opens.

7.5.4 Cold Solder The reflow profile should reach temperatures high enough to ensure that the solder melts completely and proper wetting of the land surface occurs. A cold solder can reduce mechanical integrity of the solder joint and can cause it to fail electrically or function intermittently. Optical inspection is the best way to inspect for cold solder joints.

7.5.5 Defect Correlation/Process Improvement It is important to use inspection information to control the manufacturing process to maximize quality and yield. The manufacturing process leaves a signature (acceptable or unacceptable) on each component, this signature can be observed through inspection. The signature can be observed using methods and tools discussed previously.

In many cases a visual inspection of a BGA is the first clue to any problems. An operator can look at the edge of the BGA on all four sides. The distance between the BGA and the circuit board should appear uniform and the solder balls should appear consistent in shape.

To directly observe the solder connections under a BGA, x-ray or optical inspection is necessary. These methods can be used to inspect for obvious defects such as bridges and missing balls. They are also useful for characterizing the BGA reflow process. During inspection the BGA solder balls should be examined for uniformity of size and shape. In the absence of wetting indicators, the solder balls should appear round and of equal size throughout the package. A PBGA with a 0.75 mm diameter ball prior to reflow will swell to a nominal 0.90 mm diameter after reflow; a 36% increase. A 10-15% variation in solder ball area from the center to the edge of the package is normal but a larger variation can indicate a problem with the reflow process.

X-ray inspection of the BGA from an angle is also useful to examine the shape of the BGA solder ball in the area at which it makes contact with the land. By changing the angle of x-ray inspection the land is shifted so that it does not obscure the rest of the solder ball. This allows the operator to inspect the shape of the solder connection as it forms onto the land to verify that the land is in contact with the solder ball and the solder is completely wetted to the land.

Quantitative measurement of the solder bond x-ray image can be performed using image analysis software. Such software is useful but not required for the inspection of BGAs. The advantage of the software is in its ability to identify and display subtle variations in the size and shape of the solder bond image which is not easily observed by an operator. These subtle variations are a signature of the process used to manufacture the part and can be used to monitor the process and to correct for deficiencies. A number of signatures can be correlated with known process deficiencies.

7.5.6 Insufficient/Uneven Heating A common process problem is insufficient or uneven heating of the BGA. This problem occurs more often during rework but can also be seen in production when working with multilayer boards with many ground or power planes. The problem can also occur on double-sided boards when a shielded component is on the backside near the location of the BGA. The problem results when a thermal conductor removes the heat from the BGA before complete reflow can occur. The x-ray image of this problem is characterized by a variation in the size of the solder balls at different locations under the package.

Insufficient heating is generally characterized in an x-ray image by small partially reflowed solder balls in the center or to one side of the package. Insufficient heating may also be characterized by a jaggedness around the perimeter of these solder balls; indicating that the solder partially reflowed but not long enough to completely wet to the land and collapse to a nice round ball. Misalignment of the solder ball with respect to the land is also an indicator of inadequate heating. The x-ray image of misalignment is characterized by elongated solder balls which may or may not have a consistent orientation.

X-ray inspection at a 45° angle is also a useful technique to locate signatures associated with insufficient heating or nonwetting. The solder ball should contact and completely wet to the land forming a smooth pillar. Signatures associated with insufficient heating include incomplete wetting to the land, or a waist in the solder connection indicating that the solder ball and solder paste did not flow together to form a single solder joint (see Figures 7-34 and 7-35).

7.5.7 Component Defects Component defects such as popcorning and warpage are generally caused by improper handling of the BGA component prior to reflow. Both of these problems produce a characteristic signature in the x-ray image. Popcorning causes the BGA package to expand below the die; resulting in an increase in size (and possibly bridging) of the solder balls in the center of the package as they are squished between the package and the board (see Figure 7-36).

BGA warpage is more subtle than popcorning and can be more difficult to detect in an x-ray image (see Figure 7-28). Warpage tends to be the largest at the corners of the package. The x-ray image of a warped BGA tends to have large

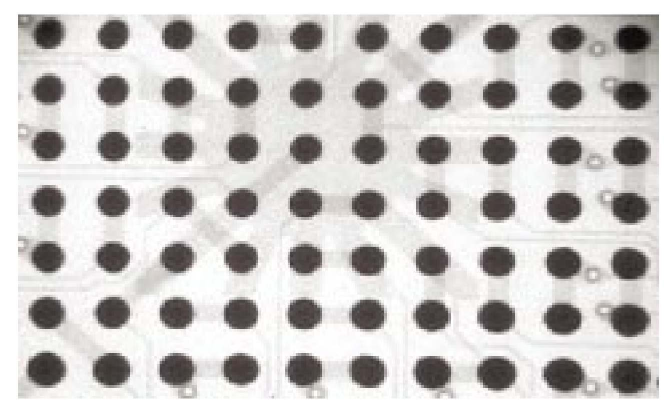


Figure 7-34 X-Ray Image Showing Uneven Heating
Note the solder balls are larger at the bottom than the top.

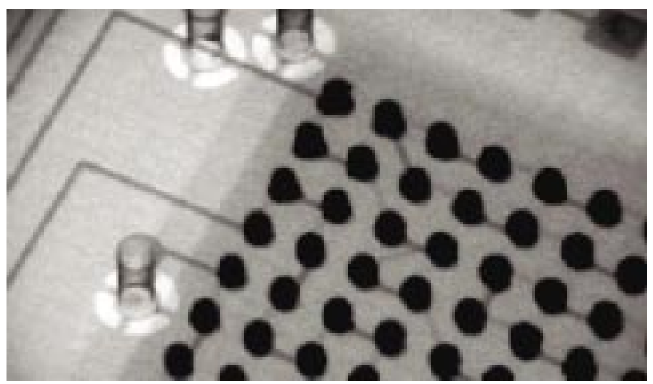


Figure 7-35 X-Ray Image at 45° Showing Insufficient Heating in One Corner of the BGA
Note the irregular shape of the solder bonds at the top of the image.

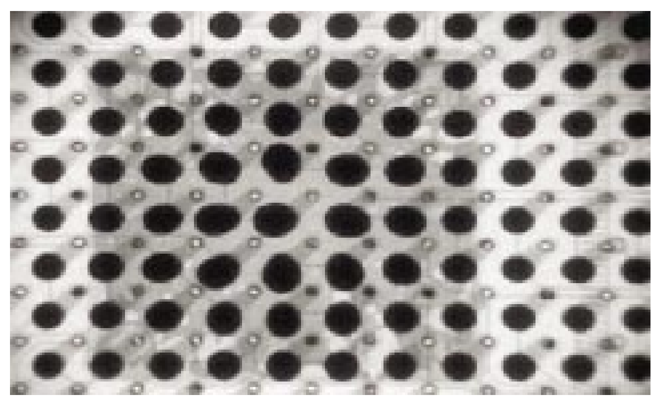


Figure 7-36 X-Ray Image of Popcorning
Solder balls in the center of the package are oversized but had not bridged.

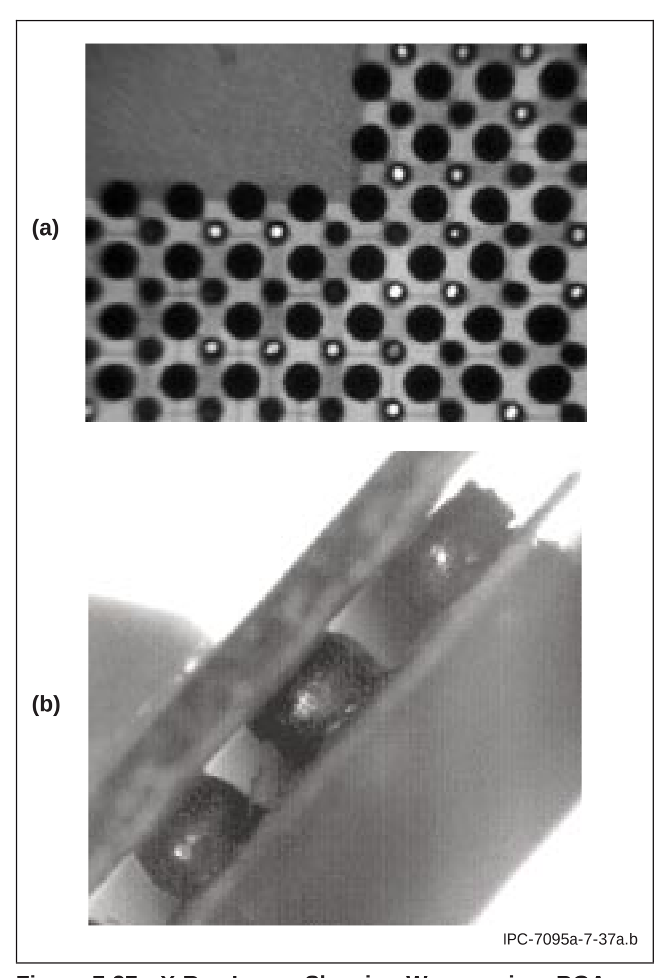


Figure 7-37 X-Ray Image Showing Warpage in a BGA
The x-ray image (a) shows a distortion of the ball bonds in the lower right corner; characterized by large elongated bonds. The same location as viewed through a visual microscope (b) shows warpage and the solder ball peaking away from the package.

elongated solder connections at the corner of the package where warpage has occurred. The illustration in Figure 7-37a shows the x-ray image and Figure 7-37b shows a video microscope image of the package. Note that in Figure 7-37b the ripple in the substrate which is characteristic of a stress relief which likely occurred during reflow.

7.6 Repair Processes

7.6.1 Rework/Repair Philosophy Ball Grid Arrays are a forgiving component package. With their self alignment characteristics a Ball Grid Array can be placed as much as 50% Ball off land and when reflowed the package will properly align itself. With a controlled process and appropriate equipment, rework should be kept to a minimum.

There are many rework systems on the market, most of which use a prism for placement which allows the viewing of the land pattern on the board with the ball image superimposed over it. Most systems also allow board preheat and stored reflow profiles for many different component sites. This section will focus on conditions that should be met in order to successfully rework a BGA.

There are three main rework functions for BGAs: removing the component, placing the component, and reflowing the component. These will be discussed in the following paragraphs.

7.6.2 Removal of BGA When removing a BGA a decision has to be made regarding whether the component will be reballed and used again or simply discarded. If the component is to be reused and it is overmolded plastic, it will have to be baked. These packages are nonhermetic and

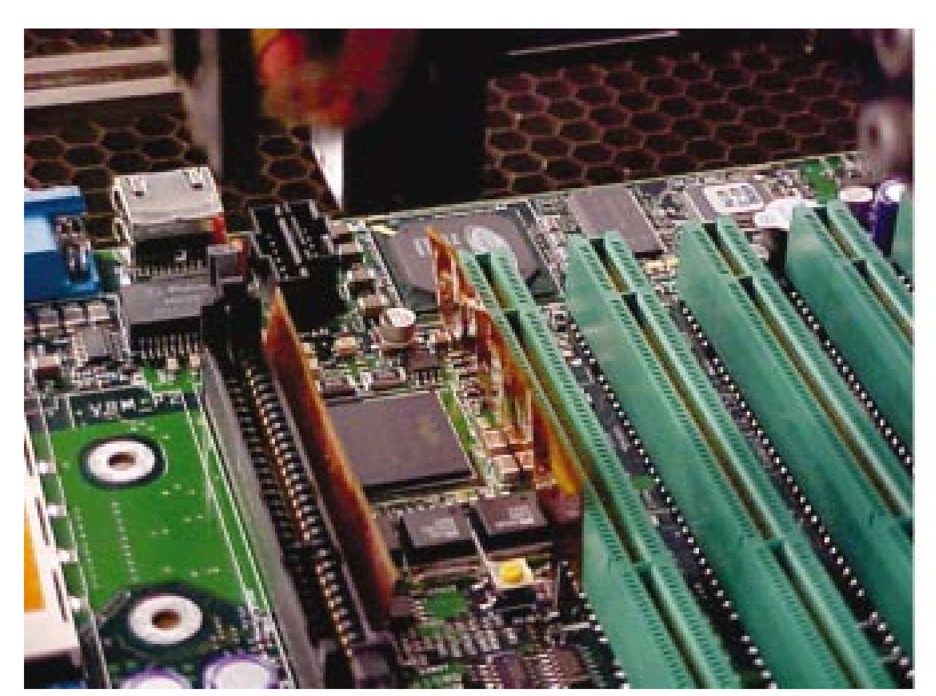
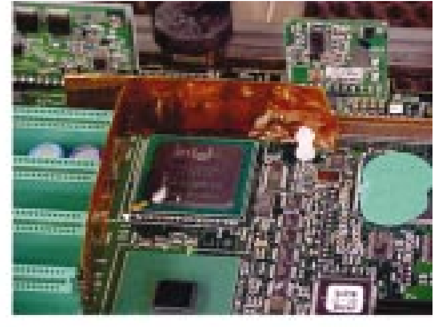
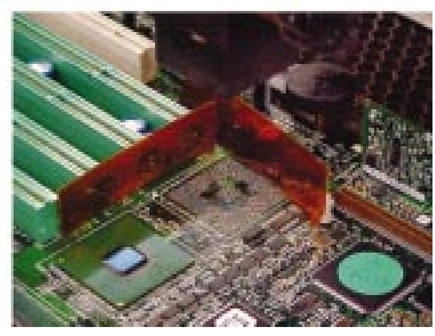




Figure 7-38 BGA/Assembly Shielding Examples

therefore absorb water. The baking process drives off moisture and prevents the ''popcorning effect'' which is water vaporizing within the component during reflow and causing catastrophic failure. Another consideration before removal concerns the components adjacent to the BGA. If hot air is used, and if the profile to be used exceeds 4°C per second the components surrounding the BGA may need to be shielded due to thermal shock or secondary reflow. Polyimide tape or water soluble mask that is commonly used in the wave solder processes can be used as shielding. See Figure 7-38 for shielding with kapton tape to prevent damage to adjacent components when using hot air for BGA repair.

7.6.3 Replacement

7.6.3.1 Site Dressing Once the BGA has been removed from the board, solder will have to be removed from the land pattern. Solder vacuums and solder wick work well for cleaning lands. Caution has to be used when using any of these because the land can lift with excessive heat or pressure. Each land must be completely flat and clean before placing the new BGA.

7.6.3.2 Flux Application (No-Clean vs. Cleanable) Two different methods of flux application can be used: paste flux or solder paste. If paste flux is to be used ensure that the solder balls are Sn63/Pb37 (eutectic). Many ceramic BGAs use Pb 90/Sn10 solder balls (noneutectic) which reflow at 302°C. If the solder balls are not Sn63/Pb37 then solder paste has to be used. If solder balls are SN63/Pb37 then liquid flux is the quickest method for reattaching a BGA. It is simply applied to the land pattern and the BGA is placed over it. One drawback of this method is the coplanarity issue. If the lands are not perfectly flat, some of the balls may not touch and oxidize before reflow is achieved. If no-clean flux is used this problem is amplified. However a nitrogen atmosphere can help improve the condition. Excessive flux application may also cause bridging between solder balls.

7.6.3.3 Paste Application Paste Application is the preferred method but it does add time to the rework process as well as tooling cost. Paste can be applied locally with the use of mini-stencils. These stencils can be purchased from many different suppliers and are tailored to fit specific land patterns. A fixture or tape can be used to hold the stencil in place during application on the land pattern. When using these methods, considerations have to be made for solder paste handling and stencil cleaning. Solder paste can also be applied to the BGA using a syringe or paste dispensing frame with other proper tooling. The amount of solder paste applied should be carefully controlled.

7.6.3.4 Rework Issues Interpackage spacing is decreasing constantly. Even if companies have some design for manufacture (DFM) guidelines for interpackage spacing, those on the front line of manufacturing know very well that DFM guidelines are not always followed. So, using ministencils to print solder paste is becoming more difficult. Also, because a ministencil is needed for each size and type of part, it not only slows down the process but also quickly adds to the cost of repair.

Ministencil is not the only issue with ever-decreasing interpackage spacing. Using different hot air nozzles for each size and type of part being removed also adds to the cost and complexity of rework. Additionally, the potential for

melting solder joints of neighboring components is a serious concern. In addition to increased intermetallic thickness because of unnecessary reflow, which weakens the solder joints, the boards must be baked before rework, increasing cycle time.

Throughput in rework is very important. Unfortunately, BGAs and some of the larger components can take at least 20 minutes per component for removal and replacement.

Another important issue in rework is PCA board warpage. Warpage partly is due to intense local heating for a relatively long time necessary to remove the component.

For BGA repair, there are two rework processes in use today: hot air and laser. Hot air is the most common. The new process for removal and replacement of surface mount components, including BGAs and CSPs, is laser based.

7.6.3.5 Hot Air Systems for BGA Repair Hot air systems are either totally manual or semiautomated. Using a nozzle, they blow hot air on the part to be reworked. The part is pulled away from the board when the solder on all joints is molten. The hot air usually is directed on the leads by a nozzle designed specifically for that component. The package body is heated by the hot air impinging on the package and conduction within the package. Initially, the package is preheated with the nozzle some distance away (typically 25 mm or more) from the package body. Then the nozzle is lowered to a point just above the package body and lead temperature increases sharply until it reaches a peak. During this process of blowing hot air, the solder joints of neighboring components even 12 mm away can reflow, an unwanted and undesirable result. With higher velocity air, smaller components such as CSPs are prone to movement during rework.

After the component is removed, paste application for reattachment is a most difficult and time-consuming process. Typically, a ministencil or dispenser is used to apply the paste. Both hot air nozzles and ministencils are needed for each type and size of part being reworked. Both these items require sufficient interpackage spacing for rework.

7.6.3.6 Laser Systems for BGA Repair The laser systems use from one to four diode lasers. Some of the laser systems are limited to reworking only peripheral components, in which the leads are in the laser's line of sight. However, there are other laser systems that use multiple diode lasers and can rework both peripheral and array type packages such as BGAs, chip scale packages (CSPs) and flip chips by rapidly scanning top of package surfaces. This causes BGA/CSP/flip chip ball to reflow underneath by conduction through the package, as is the case in hot air rework. Some of these laser systems also have a built-in automated thermal management capability to monitor and control package temperatures within the specified limits to prevent overheating. There are laser systems with or without dispensing and pick and place capabilities. There are also laser systems with or without built in temperature monitoring capability.

Because the laser beam is very narrow, components even 1 mm away do not experience any heat. Laser systems heat the package without melting the solder joints of neighboring components.

7.6.3.7 Profile Requirements Whether using laser or hot air, the reflow profile for a BGA during rework is the same as the profile for a convection oven. Preheating the board to 100°C before initiating the removal or replacement cycle should be sufficient in keeping board warpage to a minimum. These requirements are summarized in Table 7-12. Be careful not to push the preheat towards 120°C since this is where the flux typically activates. If this happens the flux could be activated before it is needed and cause poor solderability during reflow.

Flux activation is the next step in the profile. Sufficient time should be allowed for the flux to clean the ball and the land during the reflow profile. Flux should stay within 120°C to 150°C for 30 to 120 seconds. After the flux has cleaned the site, a ramp rate of 2° to 4°C can be used. The standard 2°C for SMT profiling can be amended since there should not be any heat sensitive components such as capacitors or resistors within the reflow nozzle when using

Table 7-12 Repair Process Temperature Profiles for FR-4 Material

Profile Topic	Temperature Range	Time Range
Preheat	100° - 110°C Not to exceed 120°C	N/A
Flux Activation	120° to 150°C	30 to 120 seconds
Component Ramp Rate	2° to 4°C per second	
Reflow Dwell time	Above 183°C	30 to 90 seconds
Solder joint Temp. Peak	200° to 220°C	
A moisture sensitive component max temperature	220°C	
Component Max Temp.	230°C	60 seconds
Board Temperature	Above 150°C	Not to exceed four minutes

hot air. The components that are adjacent to the nozzle should be shielded with polyimide tape or water soluble mask to protect components from thermal damage when using hot air (see Figure 7-36). The reflow dwell time should be in the range of 30 to 90 seconds with the solder joint peaking between 200°C to 220°C within this range. The balls at the center of the BGA package may exceed the 90 second recommendation due to entrapped heat from the reflow process. The board temperature should not be kept above 150°C for any longer than four minutes. This requirement is due to the glass transition temperature for FR-4.

8 RELIABILITY

Reliability is the ability of a product to function under given conditions and for a specified period of time without exceeding acceptable failure levels. The reliability of electronic assemblies requires a definitive design effort that has to be carried out concurrently with the other design functions during the developmental phase of the product. Reliability is defined in IPC-SM-785.

In the short term, reliability is threatened by early life failures due to insufficient product quality. These infant mortalities caused by defects can be eliminated prior to shipping by the use of appropriate screening procedures. Long term failures are the result of premature wear-out damage caused by inadequate designs of the assembly. The design guidelines of IPC-D-279 is a good reference.

8.1 Damage Mechanisms and Failure of Solder Attachments The reliability of electronic assemblies depends on the reliability of their individual elements and the reliability of the mechanical thermal and electrical interfaces (or attachments) between these elements. One of these interface types, surface mount solder attachment, is unique since the solder joints not only provide the electrical interconnections, but are also the sole mechanical attachment of the electronic components to the printed board and often serve critical heat transfer functions as well. A solder joint in isolation is neither reliable nor unreliable; it becomes so only in the context of the electronic components that are connected via the solder joints to the printed board.

The characteristics of these three elements - component, substrate, and solder joint - together with the use conditions, the design life, and the acceptable failure probability for the electronic assembly determine the reliability of the surface mount solder attachment.

8.2 Solder Joints and Attachment Types Solder joints are not homogeneous structures. A solder joint consists of a number of different materials, many of which are only superficially characterized. A solder joint consists of:

1. The base metal at the printed board.
2. One or more intermetallic compounds (IMC) - solid solutions of a solder constituent, typically tin (Sn) with the board base metal.
3. A layer from which the solder constituent forming the board-side IMC(s) has been depleted.
4. The solder grain structure, consisting of at least two phases containing different proportions of the solder constituents as well as any deliberate or inadvertent contaminations.
5. A layer from which the solder constituent forming the component-side IMC(s) has been depleted.
6. One or more IMC layers of a solder constituent with the component base metal.
7. The base metal at the component.

The grain structure of solder is inherently unstable. Since at room temperature, eutectic tin-lead solder is above its recrystallization temperature, the grains will grow in size over time. The grain structure growth reduces the internal energy of a fine-grained structure. This grain growth process is enhanced by elevated temperatures as well as strain energy input during cyclic loading. The grain growth process is thus to some degree an indication of the accumulating fatigue damage. This indication is significantly more pronounced for solder joints subjected to accelerated testing (more cyclic strain energy and less time-dependent growth) than for solder joints in operational use (more time-dependent growth and less cyclic strain energy).

Contaminants, like lead oxides and flux residues, reside predominantly at the grain boundaries. As the grains grow, the concentration of these contaminants is increased at these grain boundaries, therefore weakening them. After the consumption of about 25% of the fatigue life of the solder, micro-voids can be found at the grain boundary intersections; these micro-voids grow into micro-cracks after ~40% of the fatigue life; these micro-cracks grow and coalesce into macro-cracks leading to total fracture of the solder joint.

The solder joints frequently connect materials of highly disparate properties, causing global thermal expansion mismatches. Solder, as the main material, often has properties significantly different than the bonding structure materials, causing local thermal expansion mismatches. The severity of these thermal expansion mismatches, and thus the severity of the reliability threat, depends on the design parameters of the assembly and the operational use environment.

8.2.1 Global Expansion Mismatch The global expansion mismatches result from differential thermal expansions of an electronic component or connector and the printed board to which it is attached via the surface mount solder joints. These thermal expansion differences result from differences in the CTEs and thermal gradients as the result of thermal

energy being dissipated within active components. Global CTE-mismatches typically range from about 2 ppm/°C (1 ppm = 1x10^6) for CTE-tailored high reliability assemblies to ~14 ppm/°C for ceramic components on FR-4 printed boards. Figure 8-1 is showing a solder joint failure due to CTE mismatch on a wafer level CSP.

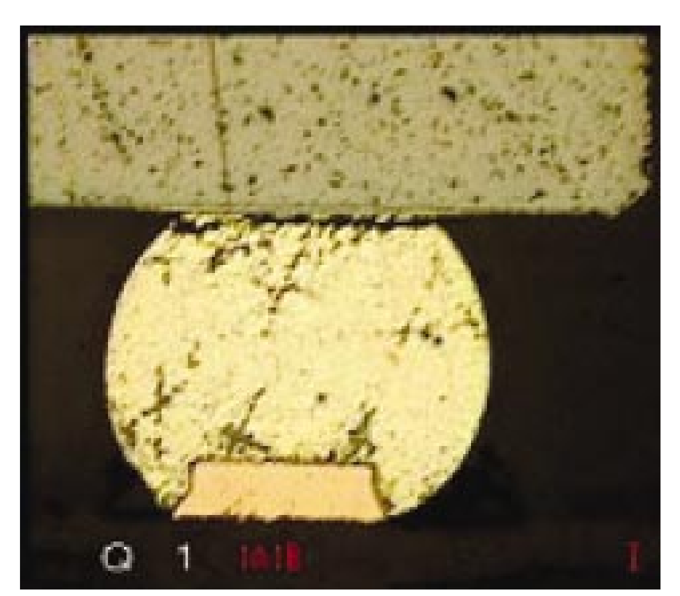


Figure 8-1 Solder Joint Failure Due to CTE Mismatch

8.2.2 Local Expansion Mismatch The local expansion mismatch results from differential thermal expansions of the solder and the base material of the electronic component or PWB to which it is soldered. These thermal expansion differences result from differences in the CTE of the solder and those of the base materials together with thermal excursions. Local CTE-mismatches typically range from ~7 ppm/°C with copper to ~18 ppm/°C with ceramic and ~20 ppm/°C with Alloy 42 and Kovar. Local thermal expansion mismatches typically are smaller than the global expansion mismatches, since the acting distance, the maximum wetted area dimension, is much smaller: in the order of hundreds of micrometers.

8.2.3 Internal Expansion Mismatch An internal CTE-mismatch of ~6 ppm/°C results from the different CTEs of the Sn-rich and Pb-rich phases of the solder. Some of the proposed lead free solders have similar CTE properties. Internal thermal expansion mismatches typically are the smallest, since the acting distance, the size of the grain structure, is much smaller than either the wetted length or the component dimension - in the order of less than 25 µm.

8.3 Solder Attachment Failure The failure of the solder attachment of a component to the substrate to which it is surface mounted is commonly defined as the first complete fracture of any of the solder joints of which the component solder attachment consists. Given that the loading of the solder joints is typically in shear, rather than in tension, the mechanical failure of a solder joint is not necessarily the same as the electrical failure. Electrically, the mechanical failure of a solder joint results, at least initially, in the occasional occurrence of a short-duration (<1 µs) high-impedance event during either a mechanical or thermal disturbance.

From a practical point of view, the solder joint failure is defined as the first observation of such an event. For some applications this failure definition might be inadequate. For high speed signals with sharp rise times signal deterioration prior to the complete mechanical failure of a solder joint might require a more stringent failure definition. Similarly, for applications which subject the electronic assemblies to significant mechanical vibration and/or shock loading, a failure definition that considers the mechanical weakening of the solder joints as the result of the accumulating fatigue damage might be necessary.

8.3.1 Solder Attachment Failure Classification There are some common BGA failure signatures. These defects could be induced during the assembly process or they could be a latent solder joint failure. These defects are the result of an inadequate assembly process, defective material or excessive mechanical stress during assembly. The defects could be a partial open, hairline crack, open joint with a full contact and partially lifted land. They are difficult to detect using conventional process verification tools such as X-ray and ICT test. They are a major reliability concern since they could be intermittent which will expand to be a catastrophic failure. Many times they will be discovered after a field failure return, and it will require more expensive destructive testing like cross section to confirm the source of the failure.

8.3.2 Failure Signature-1: Cold Solder Cold solder joint is a result of a low peak temperature during the reflow process (<190°C). The solder paste partially melts and will form a cold solder joint. The joint will have a rough BGA surface and sometimes necking at the interface to the board. The solder will appear grainy as shown in Figure 8-2 and there will be a difference between the grain structure of the BGA ball and the solder paste which indicates that the paste did not reach proper reflow temperature.

8.3.3 Failure Signature-2: Land, Nonsolderable Contamination on the PCB land will cause nonsolderable interface between the PCB land and the BGA ball. The solder will wet to the BGA ball but not to the land. There might be a partial or complete open with electrical contact. A failure with this signature could be a result of faulty nickel plating on board with Ni/Au surface finish known as ''black pad'' as shown in Figures 8-3 and 8-4. It also could be a result of PCB supplier rework process and reapplying solder mask to the BGA area.

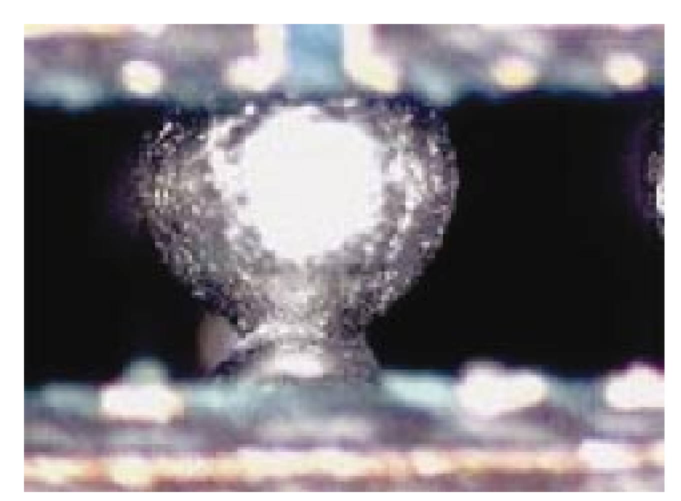


Figure 8-2 Grainy Appearing Solder Joint

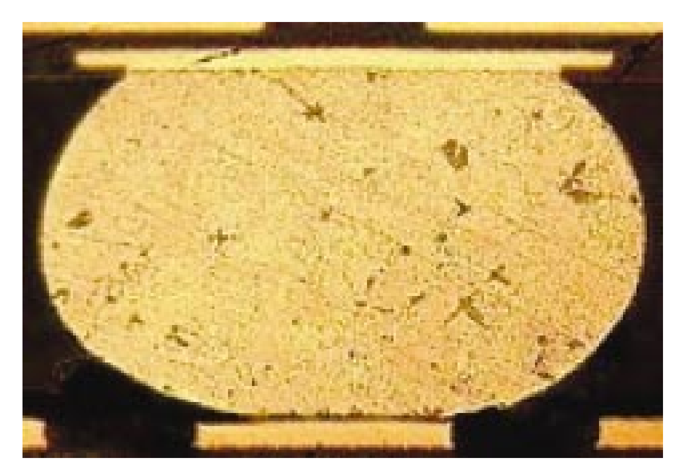


Figure 8-3 Land Contamination (Black Pad or Soldermask Residue)

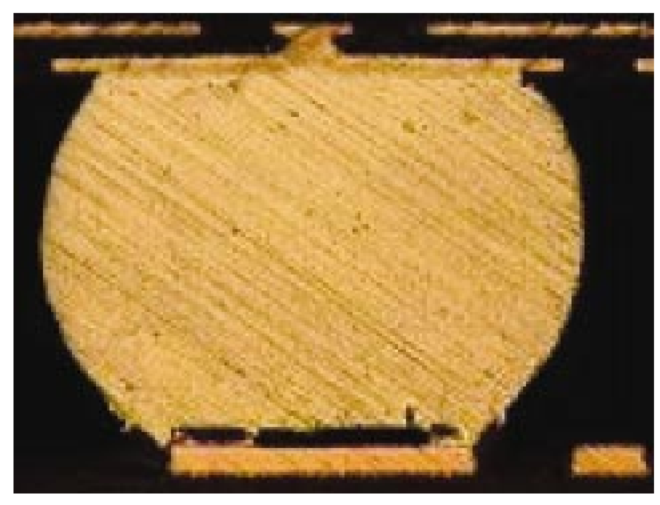


Figure 8-4 Nonsolderable Land

8.3.4 Failure Signature-3: Ball Drop This is an open solder joint which forms between the solder ball and the BGA component substrate. This causes the BGA ball to drop and creates elongated solder ball with round or a flat top. Ball drop is a failure caused by a high topside temperature during wave solder (exceeding 160°C). During wave soldering, the BGA balls are softening due to the high topside temperature. Thermo mechanical stress is causing the balls to pull away from the component substrate and create an open joint as shown in Figure 8-5.

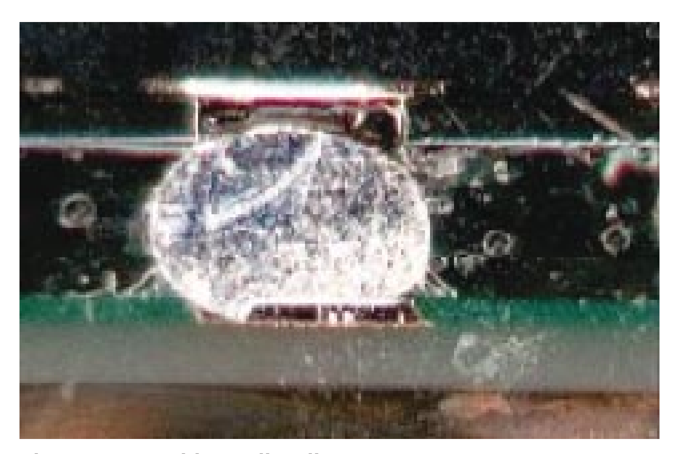


Figure 8-5 Solder Ball Pull-Away

8.3.5 Failure Signature-4: Missing Ball Missing solder ball during ball attached process or due to handling damage is shown in Figure 8-6. This defect signature is usually very clear and is easy to detect with X-ray or ICT techniques.

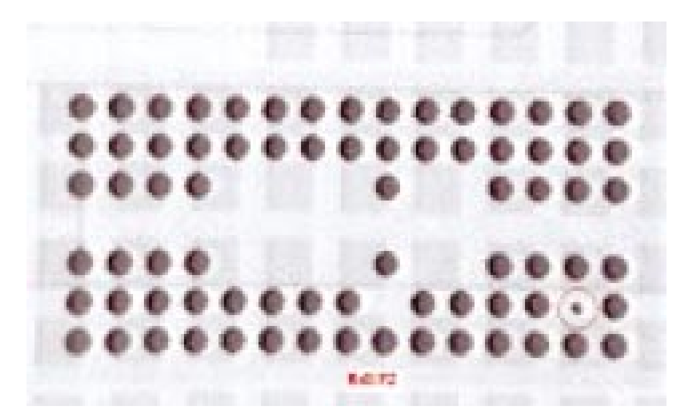


Figure 8-6 Missing Solder Ball

8.3.6 Failure Signature-5: Package Warpage This signature occurs when the BGA is warping during the reflow process. This is shown in Figure 8-7. The worst case situation is low ends package warpage (concave shape). The interface between the solder ball and the solder paste is not wetted. Both the solder paste and the BGA balls are reflowed. In some cases this signature might be associated with elongated joints (column) adjacent to the failed one.

8.3.7 Failure Signature-6: Mechanical Failure Mechanical stress caused by board flexing and in-circuit tester is not uncommon in PCB assembly. As the size of the BGA becomes larger, the stress experienced by corner joints becomes more significant. Even probing beneath and surrounding BGA had been the acceptable practice; the mechanical stress caused by the probing pins and vacuum

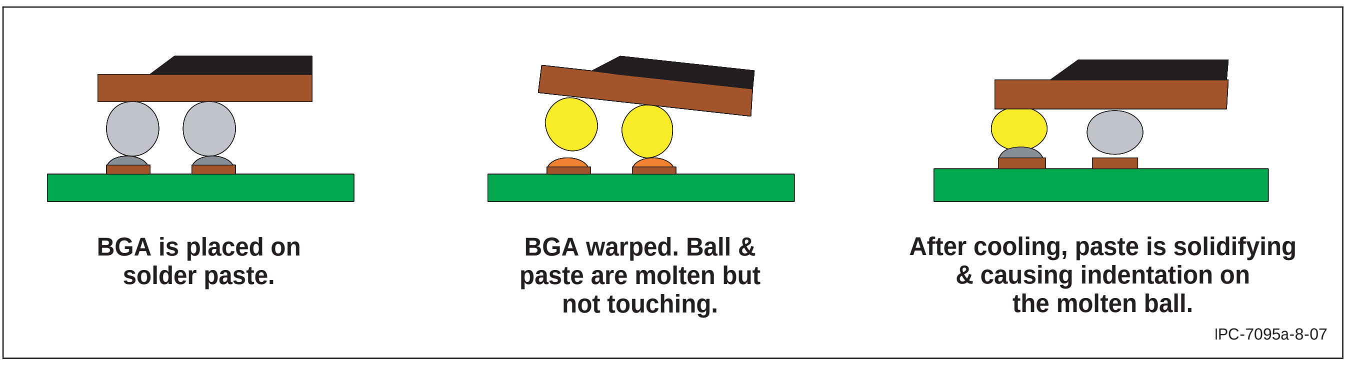


Figure 8-7 Deformed Solder Joint Due to BGA Warping

force is sometimes ignored. It is important to note that the defect induced by mechanical stresses are sometimes latent solder joint failures.

Since the weakest interface is the one that breaks, this failure signature could be different. The crack could be within the BGA ball or at the PCB or package interface or with the PCB as a lifted land (pad ''cratering''). Figure 8-8 shows a lifted corner land caused by excessive mechanical stress.

The robustness of the BGA joints against mechanical stress is a function of several factors:

- Location of the BGA
- Thickness of the PCB
- Stack Up
- Land Size
- Stiffening Mechanism
- Solder Volume

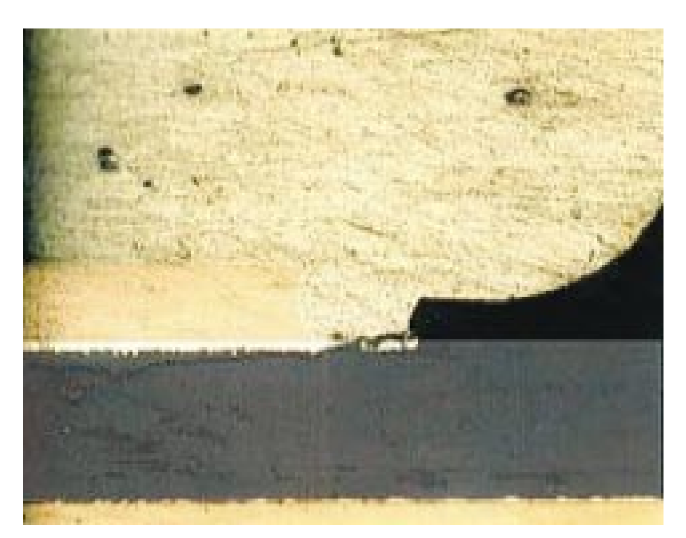


Figure 8-8 Lifted Land (Located at Corner of BGA)

As a remedy, some designers especially in the cell phone industry had adopted larger corner lands, elongate lands, and underfill to enhance robustness.

From the assembly prospective, enforcing proper fixturing and handling are keys to avoid solder joint damage.

8.3.8 Failure Signature-7: Insufficient Reflow This failure signature occurs when the BGA ball does not receive sufficient heat for the solder to become pasty. Figure 8-9 shows a classical example of the result of insufficient reflow profile; the solder ball never became sufficiently liquidous to join up with the solder on the land pattern.

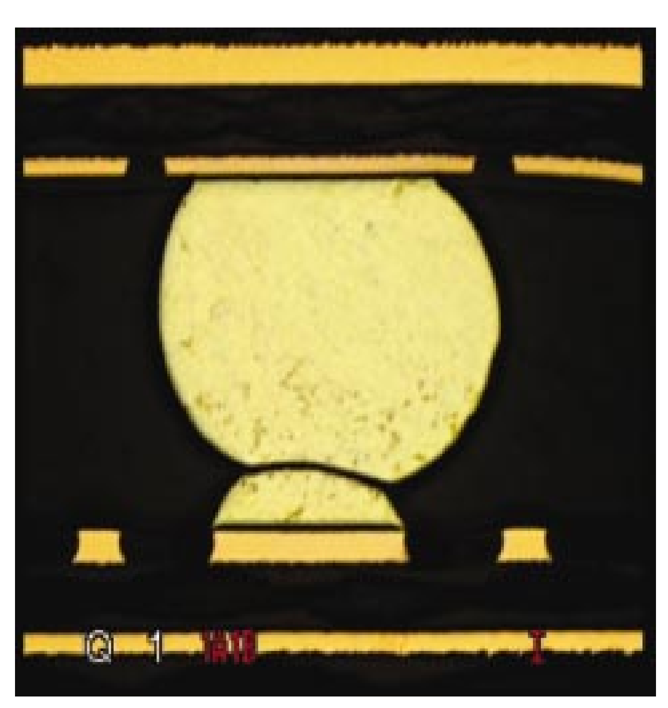


Figure 8-9 Insufficient Reflow Temperature Result Example

8.4 Critical Factors to Impact Reliability

8.4.1 Package Technology Area array components come in a variety of styles and materials. The majority of the commercial array devices utilize plastic encapsulation and a reinforced rigid organic substrate interposer material for packaging. For package-to-board interconnect, a metallized land or alloy sphere (ball) is employed. Land grid array (LGA) packaged ICs are often specified when package height is an issue while the ball grid array (BGA) uses small alloy spheres for the interconnect system. The contact alloys furnished on the majority of the plastic based

BGA is a Sn/Pb (eutectic) or a Sn/Ag/Cu (lead free) composition. Area array packages using a ceramic based substrate interposer may be supplied with high-lead solder ball or solder column, i.e., 10Sn/90Pb. A growing number of area array package variations adapt nonreinforced film dielectric for the substrate and a diverse combination of encapsulation materials. Miniature fine-pitch (FBGA) and die-size package (DSP) are also widely used (especially in portable or hand-held electronic products) and many higher power applications incorporate an in-package heat spreader or heat-spreading layer (see Section 4).

Long-term reliability of the solder attachment of the area array package, when soldered to a conventional printed board, is of primary concern. The difference in the thermal coefficient of expansion (CTE) for materials can transfer undue stress to the solder interface. The solder attachment integrity for area array packages will vary, depending on the loading conditions to which the solder joints are subjected and the reliability requirements for the product. CTE mismatch is further aggravated when large silicon die are attached to an organic substrate with a noncompliant epoxy compound. Silicon CTE is near 3 ppm/°C while the organic substrate is closer to 16 ppm/°C. Package warp during assembly processing and even the power dissipation within the package can subject the solder joints to significant tensile stresses. Excessive stress and strain at the solder interface has caused solder joint failure and even separation of the metallized lands.

When the die is attached to the package substrate with rigid epoxy, the substrate material directly beneath the die may be restricted to a CTE nearer that of the die. When solder balls are retained in the same zone and exposed to a wide variable of operating temperature, the solder interface will be subjected to excessive strain. For ‘cavity-up’ components (die attached facing away from the package substrate), only a thin dielectric layer separates the solder joints from the die. The larger the die is, the more acute the concerns for solder attachment reliability. Furthermore, the BGA solder joint fractures, when they occur, are typically near the ball-to-package interface. This is a consequence of the local expansion mismatch between the solder and the die-constrained BGA substrate.

The current trend for larger BGA package outlines is to move the contacts toward the package perimeter, with the possible exception of some thermal solder balls and vias retained at the central area of the package. Several manufacturers that cannot move the ball contact outside the die attach area have adapted a more compliant die attach material. The compliant die-to-package interface is slightly thicker and exhibits a dramatic reduction in stress at the solder-to-board interface, furnishing a substantial increase in fatigue life.

8.4.2 Standoff Height Standoff height also affects reliability of solder joints. The higher the standoff, the better is the reliability of solder joints. BGAs attached with 63Sn/37Pb solder balls result in solder joint heights that are less controlled and lower (h~400 to 640 µm), while the 10Sn/90Pb solder balls typically with diameters of 760 to 890 µm result in uniform solder joint heights of the same dimension since the 10Sn/90Pb solder has a liquidus temperature significantly above the near-eutectic Sn/Pb solders and does not melt during a typical reflow process. Table 8-1 provides information on typical standoff heights for Sn/Pb ball and solder paste metallurgy packages.

Table 8-1 Typical Standoff Heights for Sn/Pb Ball

Ball Pitches	Standoff Heights	Ball Diameter Prior to Reflow	PCB Land Size
1.27 mm	0.40 - 0.60 mm	0.75 mm	0.60 mm
1.00 mm	0.45 - 0.55 mm	0.60 mm	0.45 mm
0.80 mm	0.35 - 0.45 mm	0.30 mm	0.30 mm
0.50 mm	0.18 - 0.26 mm	0.25 mm	0.25 mm
0.50 mm	0.08 - 0.15 mm	0.17 mm	0.25 mm

Weight of the package also affects reliability of solder joint since it impacts solder joint or standoff height. The key factors that control standoff are land size, available solder volume, and the weight of the component. The lower the weight, the smaller the land size and the larger the solder volume, the higher the standoff.

8.4.3 PCB Design Considerations Another influence on reliability is the geometry of the solder joints as well as the solder land metallization. Solder masks can have a negative influence if they are used for solder mask-defined (SMD) lands with the solder mask on the metallization lands affecting the solder joint geometries. Stress concentrations created by the SMD-solder joint geometries can be the origin of solder joint failures and reduced reliability. More than that the solder mask shape and thickness could influence the reliability of the solder joint. Figure 8-10 shows crack due to stress concentration at the solder mask.

For equal solder joint height, increases in fatigue life by factors of about 1.25 to 3 can be anticipated with the use of nonsolder mask-defined (NSMD) vs. SMD lands with the larger improvements for solder joints with the more severe loading conditions [Refs. 14-18]. Surface finish also plays a critical role in BGA solder joint reliability. HASL, a commonly used surface finish may be too thick or too thin. Insufficient solder thickness may be consumed as intermetallic, which is unsolderable. Immersion gold over electroless nickel is prone to the black land defect which leads to solder joint cracking under mechanical and thermal stress. The ‘‘black land’’ defect is thought to be caused by corrosive reaction of the nickel during the gold plating process.

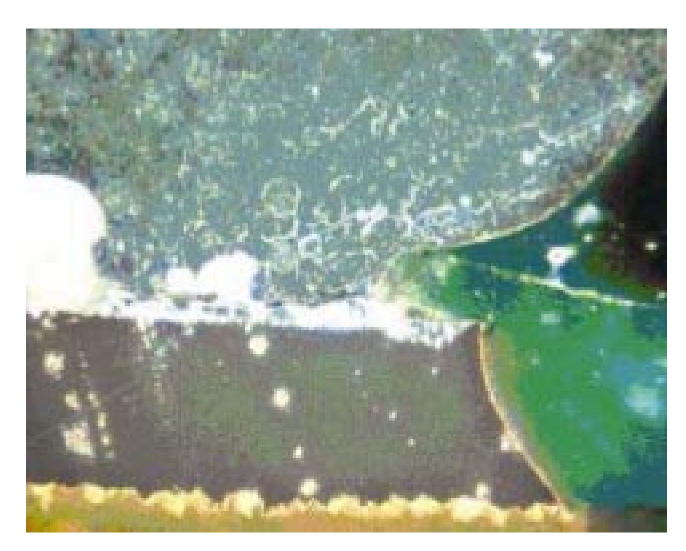


Figure 8-10 Solder Mask Influence

Laminate cracking is also a possible failure mechanism under BGA solder joint lands. Such failure is thought to be caused by thermal mechanical stress during reflow and or subsequent mechanical stresses on the joints. Via in land or via next to land may cause drainage of solder. This is generally not recommended. Via in pad is being tried by some companies with successful results. However, such an approach should be considered only by companies with extensive internal resources to validate reliability of solder joints with via in pad technology.

Microvias are becoming more common in BGA lands. Most of the BGAs will have voids whenever microvias are used. Studies showed that most voids are not a reliability risk to initiate a crack, however, they reduce the joint area and will short the time to failure when a crack is propagated. Figure 8-11 shows a failure after reliability testing where the void was so large that the ball collapsed.

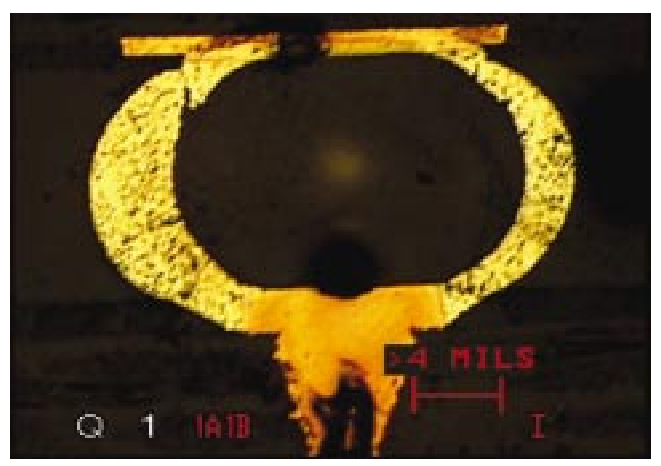


Figure 8-11 Reliability Test Failure Due to Very Large Void

8.4.4 Reliability of Solder Attachments of Ceramic Grid Array Ceramic CTE is about 6 ppm/°C; the CTE of organic-based PCBs is in the range of 16-20 ppm/°C. Thus, a global CTE-mismatch of about 10 to 14 ppm/°C exists between ceramic components and organic printed boards. To compensate for the large global CTE-mismatch, ceramic components typically require solder columns to function reliably in most applications. Since the corner joints are loaded more than other solder joints (they are farthest from the neutral point or DNP) they fail first.

The solder columns, which currently are only used for ceramic GACs, are 10Sn/90Pb columns with lengths of 1.27 to 2.29 mm that are either cast onto the CGA or are wire soldered to both the CGA and the substrate with near-eutectic Sn/Pb solder. The ratios of fatigue lives, all parameters other than the solder joint height being equal, are CBGA (0.41 mm/16 mils) : CBGA (0.76 mm/30 mils) : CGA (2.29 mm/90 mils) = 1 : 4 : 45. The height of the solder columns is limited by the requirement that the column height-to-diameter aspect ratio does not produce slender columns thus changing the loading conditions; cast columns can accommodate larger aspect ratios.

8.4.5 Lead Free Soldering of BGAs This section covers the lead free soldering of BGAs. Reasons for conversion to lead free soldering processes are first enumerated followed by description of various available lead free alloys and their selection. Board Design and Assembly Consideration for BGAs are described next with a discussion on the transition technologies that occur when converting from a tin-lead to a lead free package and assembly concluding this section.

8.4.5.1 Drivers for Lead Free Technology There are two drivers for corporations to convert their products from those containing the ubiquitous tin-lead solder to a lead-free solder. One is a legislative driver and the other is a marketing driver.

The current legislative driver for eliminating lead in electronics and electrical equipment is the Restrictions on Hazardous Substances (RoHS) Directive. The RoHS Directive states that lead, mercury, cadmium, hexavalent chromium and two brominated flame retardants cannot be present in electrical and electronic equipment that enters the market in the European Union (EU) after 1 July 2006. Currently there is no legislation in either the United States or Japan that restricts the use of lead in electronic products. There are requirements in Japan to recycle a limited number of used electronic equipment including PCs, CRTs, TVs and White Goods. There is also a new EU Directive on Waste in Electrical and Electronic Equipment (WEEE). It requires that the waste be managed and recycled according to the Directive which will take effect sometime in 2005.

The other driver is a marketing driver. Corporations are developing and introducing lead free products as a marketing initiative. Essentially, they do not want to be upstaged by competitors who could introduce lead free products before them.

8.4.5.2 Lead Free Alloy Selection Ideally, the lead free alloys selected should be drop-in replacements for the currently used tin-lead (Sn-Pb) alloys. Drop-in replacement alloys do not require any significant change in the materials, equipment and processes for package and board assembly. Unfortunately, no such drop-in replacement exists within the list of potential lead free solder alloys that are currently available.

The seminal work to select the best lead free solder alloys in existence was the three year study undertaken by the National Center for Manufacturing Sciences (NCMS). This study culminated in a report that covered the evaluation of over 79 lead free solder alloys [1].

Table 8-2 shows some of the common lead free solders that were evaluated by the NCMS group. These are listed according to their melting points. The overwhelming majority of these alloys are tin-rich alloys (>90%Sn) with Sn respectively forming binary or ternary systems with other elements such as Bi, Zn, Sb, Ag, and Cu. The melting points and the Advantages and Drawbacks for these alloy systems as well as other potential alternatives are listed in the table.

The tin-rich alloys noticeably have ~30-40°C higher melting points than eutectic SnPb solder (melting point, mp = 183°C). Alloys with lower or comparable melting points are scarce.

Some consortia around the world have selected alloys from the Sn-Ag-Cu family as the lead free solders of choice. In determining this final choice of the alloy family as well as the particular alloy compositions, many factors were considered and evaluated. These included:

- Melting temperature.
- Wettability to common component substrate and board surface finishes.
- Compatibility to common fluxes, particularly no-clean fluxes.
- Component and board reliability.
- Mechanical, electrical and thermal properties.
- Reworkability.
- Compatibility with Pb (during transition period).
- Availability from suppliers.
- Cost.
- Patent concerns.

Table 8-3 below compares the composition selected by three Consortia. The compositions are very close to each other and behave very similarly in the reflow soldering process. Further, solder alloy suppliers usually state a tolerance of ± 0.2% by weight for each elemental component of the solder, which is consistent with the ANSI J-STD-006 specification. When taking this into consideration, the alloy compositions below all overlap.

Table 8-2 Common Lead Free Solders, Their Melting Points, Advantages and Drawbacks

Alloys or Alloy Systems	Melting Point (°C)	Advantages	Drawbacks
95Sn5Sb	240	Good fatigue resistance.	Higher toxicity than Pb; high melting temperature; 8°C pasty range; poor wetting; low tensile strength.
99.3Sn0.7Cu	227	Low cost in comparison to other Pb-free solders; not prone to fillet lifting in the absence of Pb.	Reduced wettability in air, but adequate in an inert atmosphere.
96.5Sn3.5Ag	221	One of the primary choices by NCMS study; used for many years in certain applications; fatigue properties are similar to SnPb solders for some accelerated reliability test results.	Poorest wetting in reflow soldering among high-Sn alloys; though wettability still adequate for most board assembly operations.
SnAgCu	217- 220	Better creep resistance than Sn-Pb solders; fatigue properties are better than SnPb solders for some accelerated reliability test rsults.	Some compositions are patented.
SnZnBi	191-199	Closest in melting point to SnPb alloys; better strength than SnPb solders; fatigue properties are better than SnPb solders for some accelerated reliability test results.	Very susceptible to oxidation and corrosion but small amount of Al could alleviate these problems; requires special fluxes and solder processes for achieving acceptable manufacturing yields.
91Sn9Zn	199		
63Sn37Pb	183	Most widely used solder alloy.	Contains Pb
58Bi42Sn	139	One of the alloys down-selected by NCMS; presently used in low temperature applications.	Melting point is too low for computer applications; susceptible to formation of low melting ternary phase by Pb contamination.
52In48Sn	118	One of the lowest melting point solders.	Indium supplies are limited; melting point too low for computer applications; susceptible to corrosion.

Table 8-3 Comparison of Lead Free Solder Alloy Compositions in the Sn-Ag-Cu Family Selection by Various Consortia

Consortium	% Sn	% Ag	% Cu
IDEALS	95.5	3.8	0.7
JEITA	96.5	3.0	0.5
NEMI	95.5	3.9	0.6

8.4.5.3 Board Design Considerations Board Design for BGA Assembly with Lead Free Solders is generally very similar to that for presently used Tin-Lead solders. The same Design for Manufacturability (DFM) rules and guidelines should be applied for lead free boards as those used to Tin-Lead (SnPb) boards. These include consideration for component orientation, soldering, via holes, solder mask, repairability and testability. Some of these are described further below.

BGA Land Pattern Designs: As in the case of SnPb BGA soldering, the preferred BGA Land style for SnAgCu soldering is the nonsoldermask defined design as opposed to the Solder Mask Defined Land Style since it allows the maximum flexibility for the PCB designer, and less stress points are introduced to the solder joint by the solder mask.

Component Placement Location on the PCB: Since SnAgCu solders require higher reflow temperatures for component soldering, the placement location of large, temperature sensitive BGA components may need to be addressed carefully. The regions near the edges of the board are, depending on the board size, thickness and layer count, typically 5 to 15°C higher in temperature than those in the central locations. Since large packages are more prone to moisture and thermal stress induced defects when subjected to higher reflow temperatures, such packages, if possible, should be confined to the central regions of the board. Other factors, such as trace routability and density, may make it necessary to place large BGAs at the edges of the board. In such cases, the reflow soldering process window will be narrowed to keep the maximum temperature the BGA components are exposed to below acceptable limits.

8.4.5.4 Reflow Soldering Considerations Reflow soldering is commonly done in an oven with heated air convection. Despite the higher reflow temperatures necessary to melt the SnAgCu solders when compared with the SnPb solders, no new equipment is necessary for lead free reflow soldering. The same ovens as used before for SnPb solders can be used with the obvious increase in the settings for the various heating zones in the reflow oven.

The environment in the oven can be either air or inert, such as nitrogen. For lead free soldering, to minimize the oxidation of the materials on the board assemblies during the high temperature reflow operation, an inert atmosphere is strongly recommended. Some board surface finishes, such as Organic Solderability Preservations (OSP) on copper may require an inert atmosphere during reflow soldering to attain acceptable solder joint yield levels.

A reflow solder profile is typically developed for all board assemblies. Since SnAgCu lead free solders require higher reflow soldering temperatures, it is very important to determine the temperature at various different locations on a board. Component temperatures may vary because of surrounding components, location of part on the board, and package densities.

To avoid moisture and thermo-mechanical stress induced failures on plastic components, it is best to measure the temperature of the component body and check to ensure that it doesn't exceed the maximum temperature it is rated for. Hence, thermocouples, which are generally used to measure the temperatures during reflow profiling, should be attached at the solder joint as well as the body of the various components during reflow profiling of board assemblies. Large components generally have greater than 5°C difference between the leads/solder balls and the molding compounds of the component.

A typical SnAgCu lead free reflow profile is compared with a SnPb reflow profile for a BGA solder joint in Figure 8-12 below.

Four different regions of the reflow profile are shown: the Preheat region during which the low melting volatile ingredient in the solder paste vehicle are evolved; the Soak region which enables the temperature to start equilibrating across the board and to start to activate the flux; the Reflow region where the solder melts, wets the land surface and forms the solder joint; and finally the Cool down stage, where the solder solidifies and the board assembly exits the oven to be cooled down by forced air blown down on the board by fans.

The profiles illustrated in Figure 8-12 are termed ''soak'' profiles since they have a soak zone before the solder is reflowed. Alternatively, ''ramp'' profiles can also be developed which contain a continuous ramp from the preheat zone to the reflow soldering zone. These ramp profiles increase the throughput of the board assemblies in the reflow ovens. But, care should be taken to avoid overheating of components, particularly on the edges of the boards.

8.4.5.5 Appearance of BGA Lead Free Solder Joints The BGA package body obscures its solder joints. However, with the help of special microscopes such as the endoscope, peripheral solder joints can be viewed. SnAgCu solder joint microstructures are multiphase microstructures and the surface of the solder joints appears rough. Figure 8-13 shows a typical SnAgCu BGA solder joint. This is much different from typical SnPb BGA solder joints which usually have a shiny surface.

8.4.5.6 Transition Lead Free Technologies The transition from a total SnPb soldering system to a total lead free

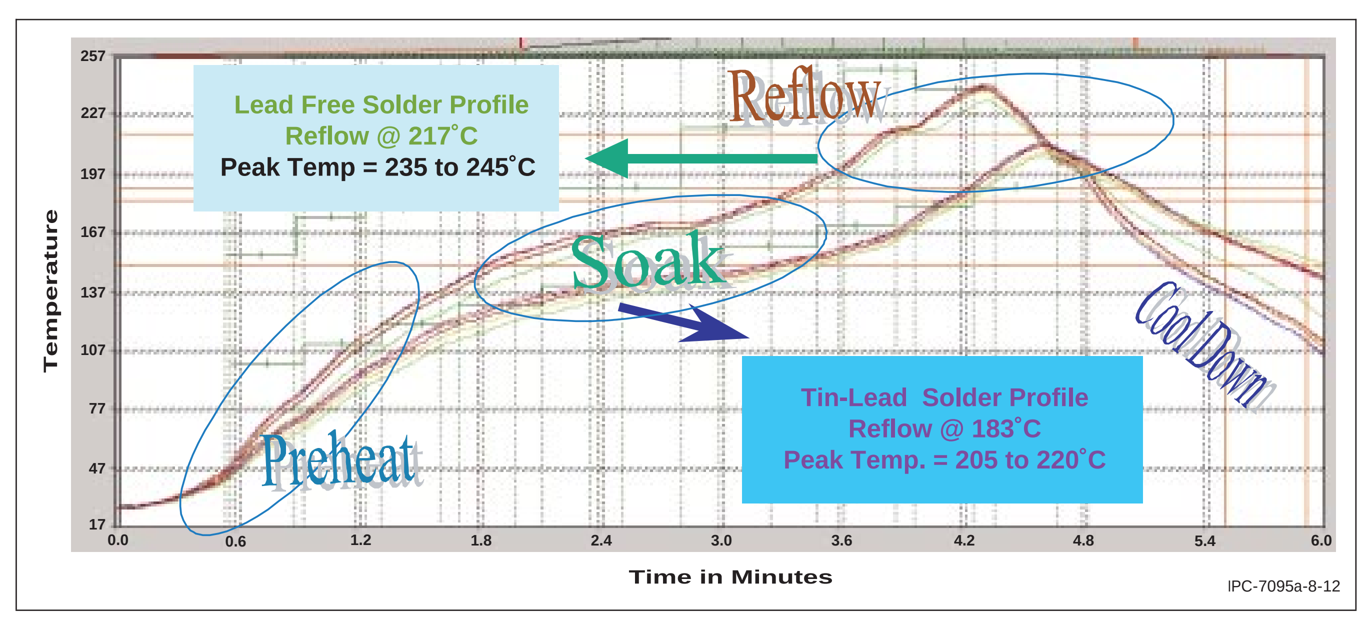


Figure 8-12 Comparison of a Lead Free (SnAgCu) and SnPb BGA Reflow Soldering Profiles Void

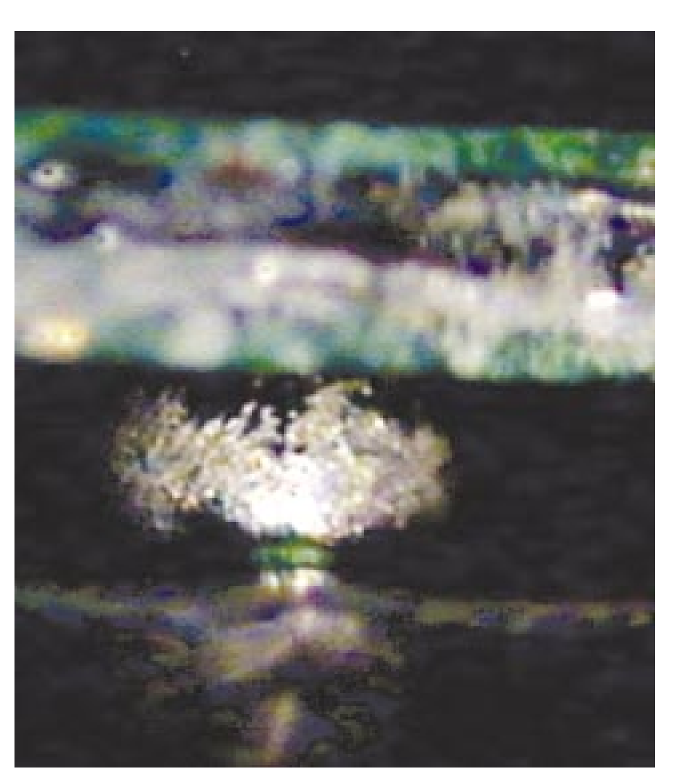


Figure 8-13 Endoscope Photo of a SnAgCu BGA Solder Ball

soldering system is not going to happen overnight. There will be an interim phase where SnPb and lead free solders will co-exist on board assemblies because the timing and the technology readiness in the various sectors of the Electronic Manufacturing Industries are not in sync. This transition phase entails that the impact of Pb in the SnAgCu solder be evaluated for impact on solder joint yields and reliability.

The various Lead Free Board Assemblies possible during this transition phase are listed in Table 8-4.

The first possible Lead Free Board Assembly listed above is Forward Compatibility. The board assembly soldering process for Forward Compatibility assemblies has been converted to lead free technology with a change in the solder paste composition and the reflow soldering profile to match this change. However, some components, such as BGAs that are soldered on the board will still have SnPb solder due to the component supplier's lead free roadmap having a conversion date later than the board assembler's conversion date. This results in the SnPb solder joints of the BGA-type components being 'contaminated' by the Pb replacement metals in the lead free solder paste.

The second possible lead free board assembly listed above is backward compatibility. Backward compatibility scenarios arise when component suppliers introduce the lead free components, but not all board assemblers that use these components have converted their board assembly lines to lead free technology. These assemblers will still be soldering the lead free components with the ubiquitous

Table 8-4 Types of Lead Free Assemblies Possible

Definition	Component Termination	Solder Paste	Board Surface Finish
Forward Compatibility	Contain Pb	Pb Free	May Contain Pb
Backward Compatibility	Pb Free	63Sn37Pb	May Contain Pb
Total Lead Free	Pb Free	Pb Free	Pb Free

eutectic Sn-Pb solder paste using Sn-Pb reflow soldering profiles. A SnPb component would obviously be preferable in this case, but the component suppliers may, due to economic reasons, not want to carry two component line items, one Sn-Pb and one lead free, for the same device. The solder joints formed with this combination of materials will have Pb ''contamination'' in the Pb-free solder balls for BGA type components.

When soldering a Ball Grid Array package with SnAgCu lead free solder balls using SnPb solder paste, two different scenarios arise based on the reflow profile used. The two reflow profiles compared are shown in Figure 8-14 with the Total Lead Free Reflow profile also shown for comparison.

The SnPb reflow profile, which is illustrative of the profile used today for SnPb assemblies, does not exceed the melting point of the BGA's SnAgCu solder ball. This causes an impact to solder joint yield and reliability.

The SnPb solder paste deposited on the lands of the solder balls melts but the SnAgCu solder balls are still not molten. The lead diffuses through the grain boundaries of the still solder ball. How high the Pb from the SnPb solder diffuses up the SnAgCu solder ball will depend on how high the reflow temperature gets and for how long the SnPb solder is molten. As shown in Figure 8-15, which depicts a micrograph of a cross-section of a SnAgCu solder ball of a BGA package soldered to a board using the standard SnPb profile, the resulting solder joint microstructure is inhomogeneous and unstable. This deleteriously impacts the solder joint reliability.

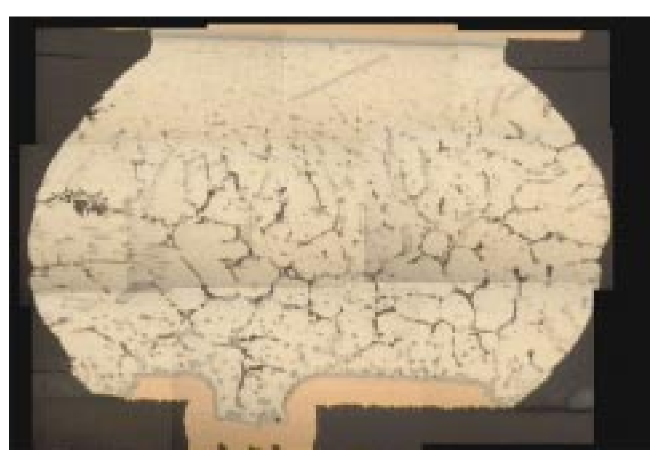


Figure 8-15 Micrograph of a Cross-Section of a BGA SnAgCu Solder Ball, Assembled onto a Board with SnPb Solder Paste using the Standard SnPb Reflows Soldering Profile. The SnAgCu Solder Ball does not Melt. Black/Grey Interconnecting Fingers are Pb Rich Grain Boundaries; Rod Shape Particles are Ag_3Sn IMCs, Grey Particles are Cu_6Sn_5 IMCs.

Yield impact on such solder joint is also deleterious due to two reasons. One is due to the poor self-alignment of the BGA during reflow soldering because the solder ball does not become molten. This creates a potential for open joints when the component is misaligned to some extent during or after the Placement process step. Secondly, the lack of ''Ball Collapse'' may cause open solder joints from a lack of contact between the solder paste deposit and the solder ball.

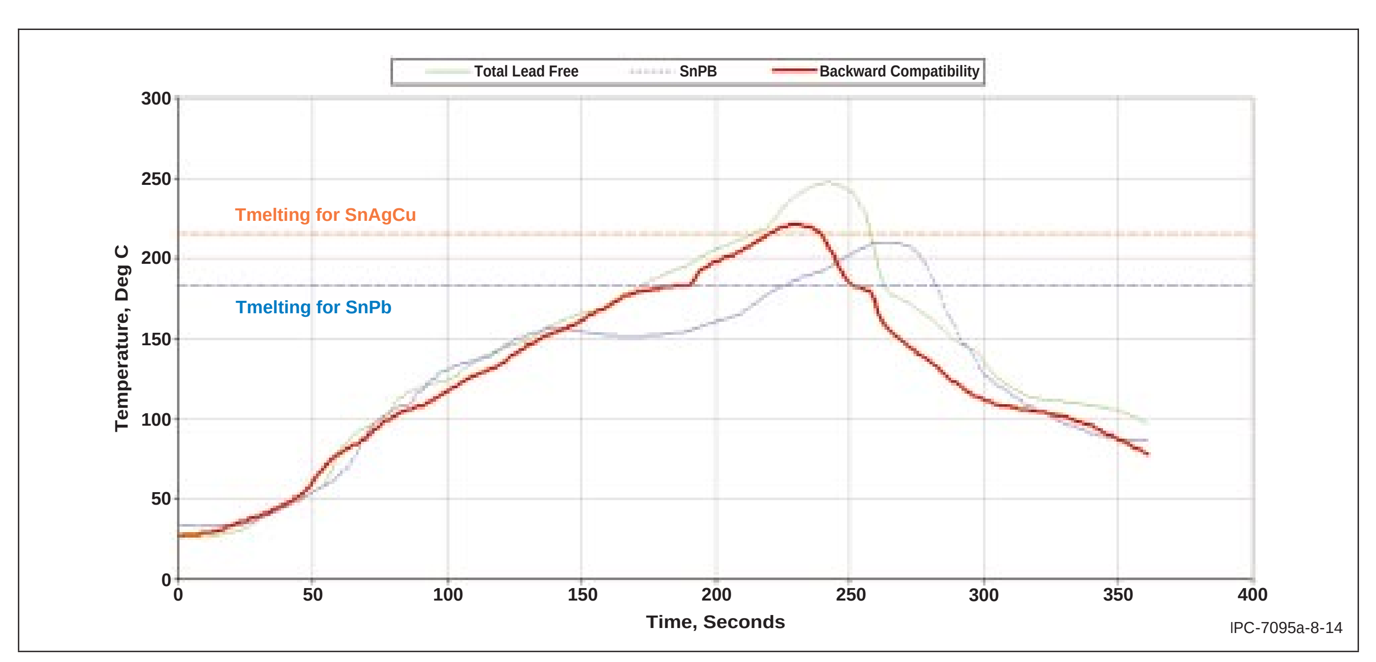


Figure 8-14 Comparison of Reflow Soldering Profiles for SnPb, Backward Compatibility and Total Lead Free Board Assemblies

Hence, for better solder joint yields and solder joint reliability, the Backward Compatibility reflow soldering profile depicted in Figure 8-14 should be used. During this reflow profile, the SnAgCu solder ball also melts, and Pb from the molten SnPb solder paste mixes thoroughly with molten SnAgCu solder ball and generates a homogeneous, refined structure of a Pb rich phase in the Sn matrix. Such a microstructure is shown in Figure 8-16.

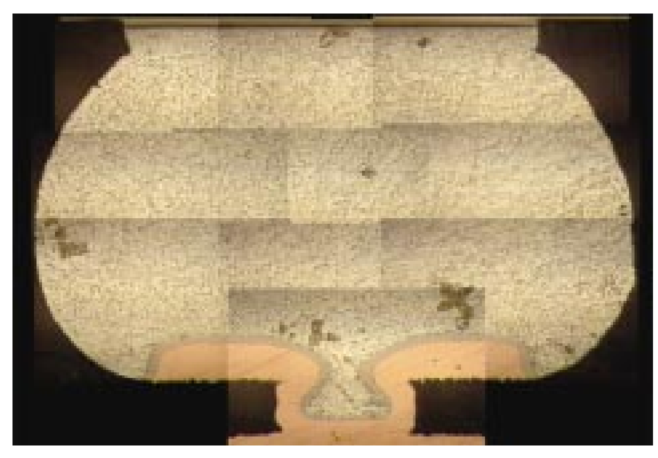


Figure 8-16 Micrograph of a Cross-Section of a BGA SnAgCu Solder Ball, Assembled onto a Board with SnPb Solder Paste using a Backward Compatibility Reflows Soldering Profile. The SnAgCu Solder Ball has Melted.

Moreover, since the SnAgCu solder ball melts and collapses, the self-aligning process and coplanarity reduction also occur, thereby enhancing solder joint yields of the BGA.

8.5 Design-for-Reliability (DfR) Process Appropriate DfR measures to improve reliability for grid array components take one of two forms, which are best employed in combination for improved reliability margins. These measures are:

1. CTE-tailoring to reduce the global expansion mismatch.
2. Increasing attachment compliancy to accommodate the global expansion mismatch by increasing the solder joint height (standoff).

Further, a DfR procedure aiming at high-reliability could also include:

3. Eliminate the effect of the global expansion mismatch by mechanically coupling the component and the substrate with an appropriate underfill.
4. Choosing a soft die attach to reduce the impact of the low die CTE (2.7 to 2.8 ppm/°C) on both the global and local thermal expansion mismatch.

CTE-tailoring involves choosing the materials or material combinations of the multilayer board and/or the components to achieve an optimum CTE. An optimum CTE for active components dissipating power is ~1-3 ppm/°C (depending on the power dissipated) with the multilayer board having the larger CTE, and 0 ppm/°C for passive components. Of course, since an assembly has a multitude of components, full CTE-optimization cannot be achieved for all components - it needs to be for the components with the largest threat to reliability. For military applications with the requirement of hermetic and thus ceramic-components, CTE-tailoring has meant the CTE-constraining of the multilayer boards with such materials as Kevlar™ and graphite fibers, or copper-Invar-copper and copper-molybdenum-copper planes. Such solutions are too expensive for most commercial applications for which glass-epoxy or glass-polyimide are the materials of choice for the multilayer boards. Thus, CTE-tailoring has to take the form of avoiding larger size components that are either ceramic (CGAs, MCMs), plastic with Alloy 42 leadframes (TSOPs, SOTs [Ref. 19]), or plastic with rigid bonded silicon die (PBGAs).

Increasing attachment compliancy for leadless solder attachments means increasing the solder joint height (C4, C5, shimming, gluing [Refs. 20, 21], 10Sn/90Pb balls, 10Sn/90Pb columns) or switching to a leaded attachment technology. For leaded attachments increasing lead compliancy can mean changing component suppliers to those having lead geometries promoting higher lead compliancy or switching to fine-pitch technology.

The DfR-process needs to emphasize a physics-of-failure perspective without neglecting the statistical distribution of failures. The process might involve the following steps:

A. Identify Reliability Requirements – expected design life and acceptable cumulative failure probability at the end of this design life.

B. Identify Loading Conditions – use environments (e.g., IPC-SM-785) and thermal gradients due to power dissipation, which may vary and produce large numbers of mini-cycles (Energy Star).

C. Identify/Select Assembly Architecture – part and substrate selections, material properties (e.g., CTE), and attachment geometry.

D. Assess Reliability – determine reliability potential of the designed assembly and compare to the reliability requirements using the approach shown here, a ‘Figure of Merit’-approach [Ref. 22], or some other suitable technique; this process may be iterative;

E. Balance Performance, Cost and Reliability Requirements.

8.6 Validation and Qualification Tests The validation and qualification tests should follow the guidelines given in IPC-SM-785, Guidelines for Accelerated Reliability Testing of Surface Mount Solder Attachments. However, for large components with significant heat dissipation, for

components of asymmetric construction, and for small global CTE-mismatches, temperature cycling tests are inadequate to provide the required information; full functional cycling including external temperature and internal power cycling is necessary.

8.7 Screening Procedures

8.7.1 Solder Joint Defects The solder joint defects of greatest reliability concern are those involving inadequate wetting for whatever reason. Properly wetted solder joints have adequate strength even for severe mechanical loading conditions as well as no diminished thermal cyclic fatigue reliability. However, solder joints not properly wetted, can prematurely fail both as the result of mechanical and thermal cyclic loading [Refs. 23, 24].

Voids in the solder joints are generally regarded as not constituting a reliability threat [Ref. 26]. Possible exceptions are large voids reducing the solder joint cross-section enough to reduce a required thermal heat transfer function, and voids in high-frequency applications where the voids can cause signal deterioration.

BGA components having noncollapsible balls (high temperature solder 90% Pb 10% Sn, with a melting point of 302°C) typically will have few or no induced voids because the ball solder never melts during the reflow profile.

8.7.2 Screening Recommendations Effective screening procedures need to be capable of causing the failure of latent solder joint defects, i.e., weak inadequately wetted solder joints, without causing significant damage to high quality solder joints.

The best recommendation is random vibration (6-10 grms for 10-20 minutes), preferably at low temperature, e.g., 40°C. This loading does not damage good solder joints, but overstresses weakly bonded ones [Ref. 26].

Thermal shock can also be sucessfully used, however some damage to good solder joints can be expected, particularly for larger components.

9 DEFECT AND FAILURE ANALYSIS CASE STUDIES

The following clauses identify possible assembly anomalies related to the assembly of BGA components. The descriptions include post process failures related to the mounting structure characteristics and the variation in the solder ball used as the BGA termination. In many instances attachment metallurgy are discussed especially if the characteristics contributed to the joint failure. Final joint configurations are also analyzed.

9.1 Soldermask Defined BGA Conditions There are two ways BGA Lands are defined: solder masked defined (SMD) where the land size is larger than solder mask and the molten BGA ball touches the solder mask after reflow. The other method for designing the BGA land is called etched or non solder mask (NSMD) defined where the mask opening is larger than the copper land and hence the ball does not touch the solder mask after reflow. This condition is shown in Figure 9-1.

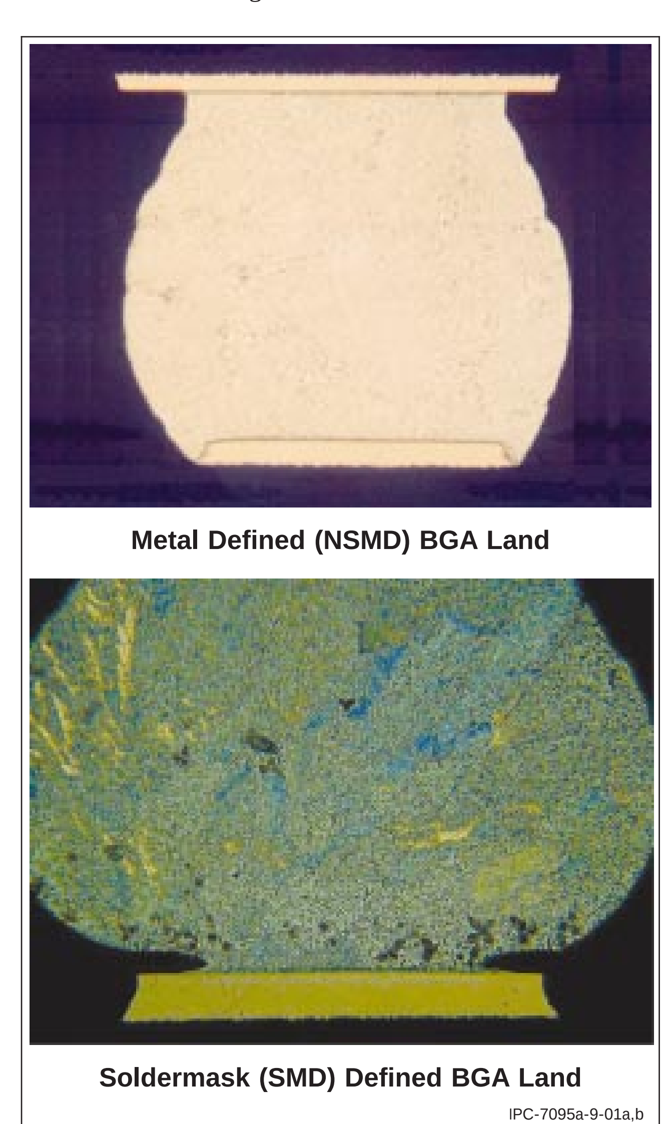
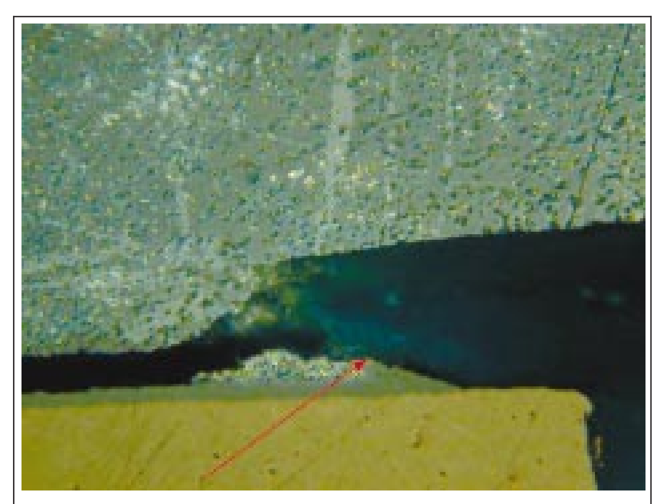


Figure 9-1 Soldermask Defined and Nondefined Lands

The main disadvantage of solder mask defined land is that the stress concentrations created by SMD (solder mask defined) solder joint can be the origin of solder joint failures and reduced reliability. This condition is shown in Figure 9-2.

For equal solder joint height, increases in fatigue life by factors of about 1.25 to 3 can be anticipated with the use of nonsolder mask defined (NSMD) versus SMD lands, with the larger improvements for solder joints with the more severe loading conditions.

9.2 Over-Collapse BGA Solder Ball Conditions The plastic BGA, generally, has solder balls that collapse to



Crack starts in the solder and eventually travels down to and through the intermetallic layer. Nickel buildup under the soldermask is also evident.

IPC-7095a-9-02

Figure 9-2 Soldermask Defined BGA Failures

about 625 µm from its original size of 750 µm. After the package is soldered to the board, the ball collapses to about 500 µm. However, if there is heat spreader or heat slug in the package for heat dissipation, depending upon the weight of the heat slug/spreader, the ball may collapse to as low as 300 µm (see Figure 9-3).

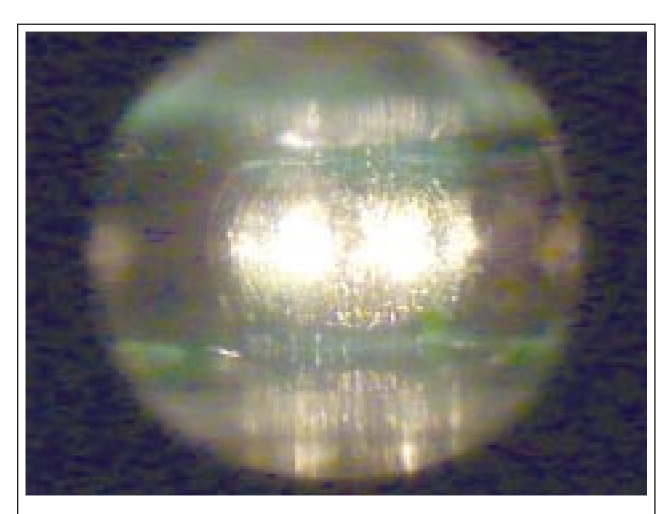
As the ball flattens there is a decrease in reliability due to limited solder height and solder joint compliancy. Also solder ball spread may occur beyond the desirable pitch clearance. A good approximation is that the initial reflow reduces the height by about 10%; with the added weight of a heat spreader this figure may increase to 25% of the original height (ball diameter). The land pattern and soldermask clearance also play a part in the analysis. Figure 9-4 shows the extremes of this condition.

9.3 Critical Solder Paste Conditions The amount of solder paste deposited for plastic BGA attachment is helpful, but not very critical in formation of good solder joint since the ball itself can be the source of solder. However, in the case of ceramic BGA (CBGA), it is very important that enough solder paste is deposited. The recommended volume of solder paste for 890 µm CBGA is 0.12 cubic mm and 0.08 cubic mm minimum. If sufficient solder paste is not deposited, as shown in Figure 9-5, the reliability of solder joint may be questionable.

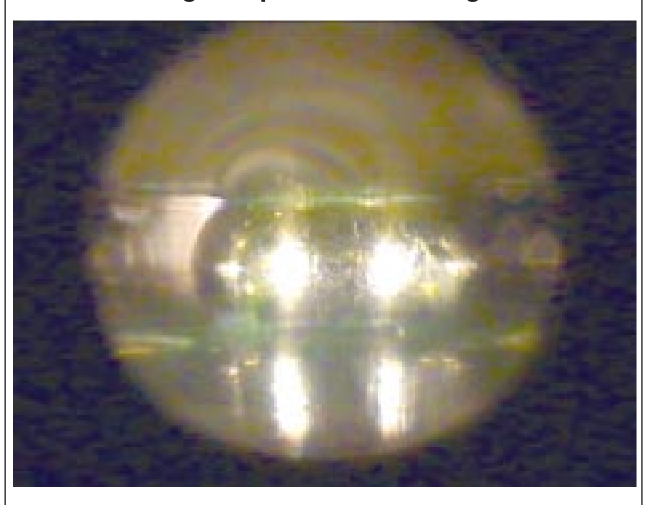
The reason solder must be added to the high temperature solder ball or column is that there is no contribution of solder volume from the package termination to the solder joint.

9.4 Void Determination Through X-Ray and Microsection Transmission X-ray can detect void presence (light areas) and the associated X-Y location. The technique can also detect uneven or missing solder balls (various dark image diameters). Figure 9-6 shows an example of this condition. However cross-section X-ray is required to determine the vertical (Z axis) location of the void in the solder joint.

There are many reasons for formation of voids in BGA. Examples of causes can be related to design (or any kind of via in the BGA land) or related to process issues, such as reflow profile, types of solder paste, and board materials. However, the presence of voids does not pose any reliability risks. Even as large a void (balloon) as that shown in Figure 9-7 can survive 1000 thermal cycles when the cyclic behavior is between 0 to 100°C, although the more common are voids shown in Figure 9-6. Even though voids



BGA Ball Shape Without Heat Slug 500 µm Standoff Height



BGA Ball Shape With Heat Slug 375 µm Standoff Height

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Figure 9-3 Over Collapsed BGA Solder Ball

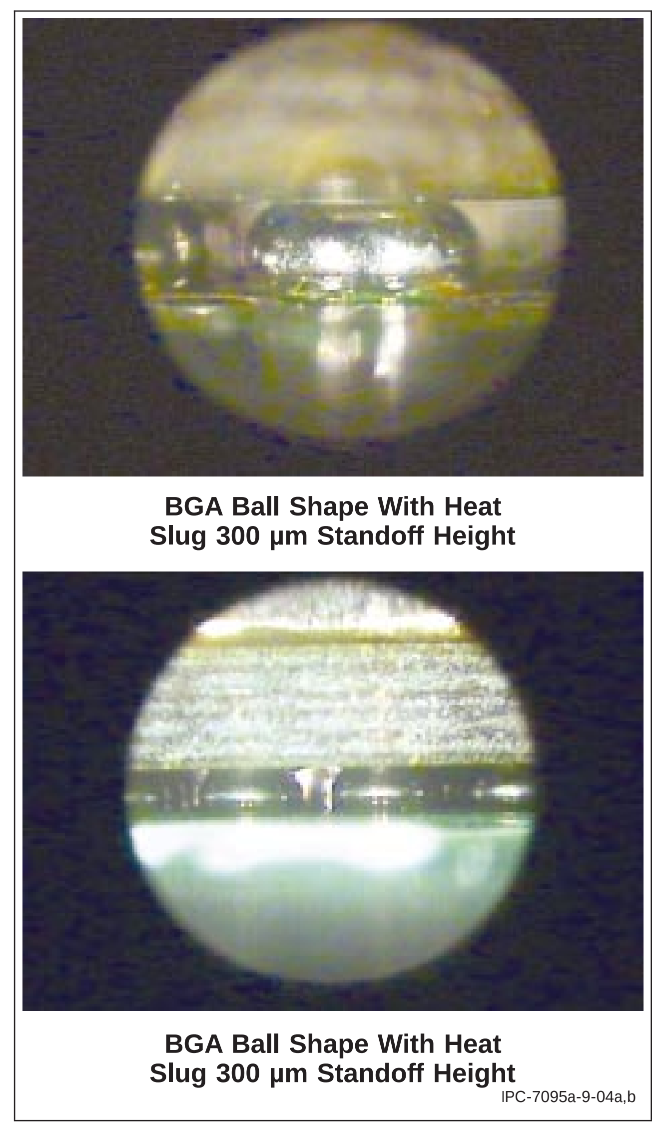


Figure 9-4 Extreme Collapsed Solder Ball Joints

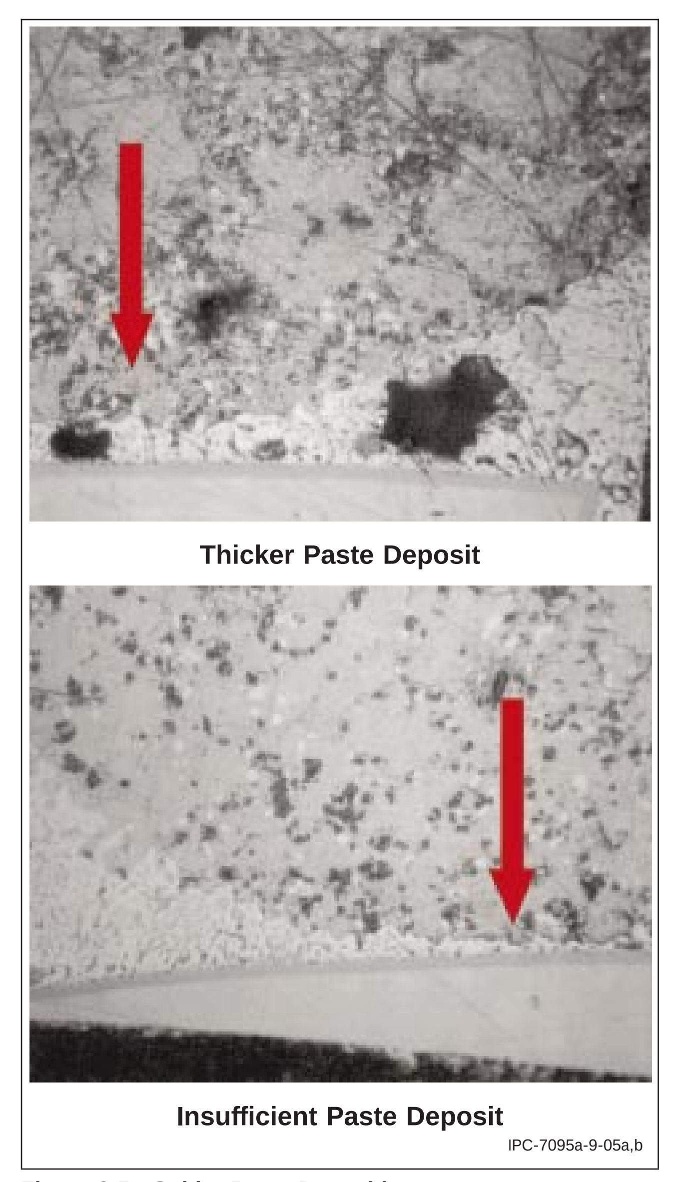


Figure 9-5 Solder Paste Deposition

do not pose reliability concerns, excessive presence of voids is an indication of design or process problems.

Reliability is related to where the product will be used. Thermal cycling is intended to demonstrate a specific application and that the product will survive that exposure.

9.5 BGA Interposer Bow and Twist Plastic BGAs have a tendency to warp during normal assembly reflow processes. The warpage can occur on the BGA substrate or on the product board to which the BGA is mounted. The result can be an open or short condition at the solder joint that deals with the stresses. The temperature (reflow profile), BGA construction, solder paste volume, and cooling condition all contribute to the possible defect.

Shorts in the corner balls, is an indication of warpage in BGA where the corners of the BGA package are bent inward (frowning BGA).

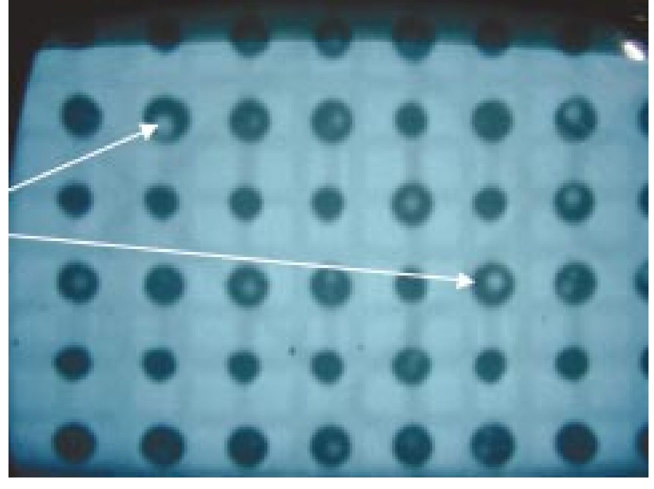


Figure 9-6 Voids and Uneven Solder Balls

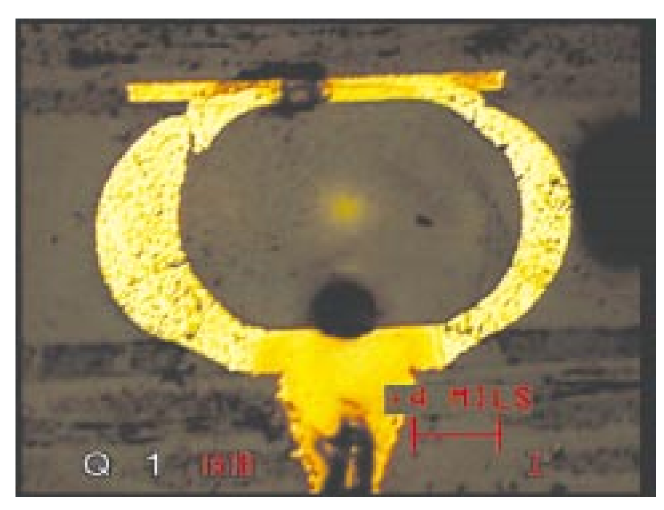


Figure 9-7 Eggshell Void

Solder shorts are caused in adjacent and/or opposite BGA corners as the substrate bows downward (frowning) and applies a stress to the corner balls. This same phenomena can cause balls, away from the corner, to lift away from the mounting substrate as the substrate changes from frowning to smiling (see Figure 9-8).

Opens in corner balls is an indication of warpage in BGA where the corners of the package are lifted upward. Such opens, as shown in Figure 9-9, could be minimized by use of solder paste on the excess side.

Adding excess solder is a band-aid and not a real solution to the problem. Determining the root cause and addressing the reasons for the anomaly is more important toward establishing a robust process. The use of excess solder paste (redesign of stencil apertures) necessitates a condition that the reflow process has already been optimized. Also the root cause cannot be eliminated such as BGA package cannot be redesigned, BGA interposer cannot be redesigned, and product board cannot be redesigned. In addition, the anomaly must consistently occur, not just as a random event. Inventory and many other conditions play a role in the determination to use the excess solder to correct the deficiency. There are times that the solution to one bad condition creates six others (solder bridging, solder balling etc.).

9.6 Solder Joint Conditions The following sections deal with the conditions of the solder ball in relationship to the mounting structure and the component interposer. In each instance, an explanation is provided as to the reason for the occurrence of the condition.

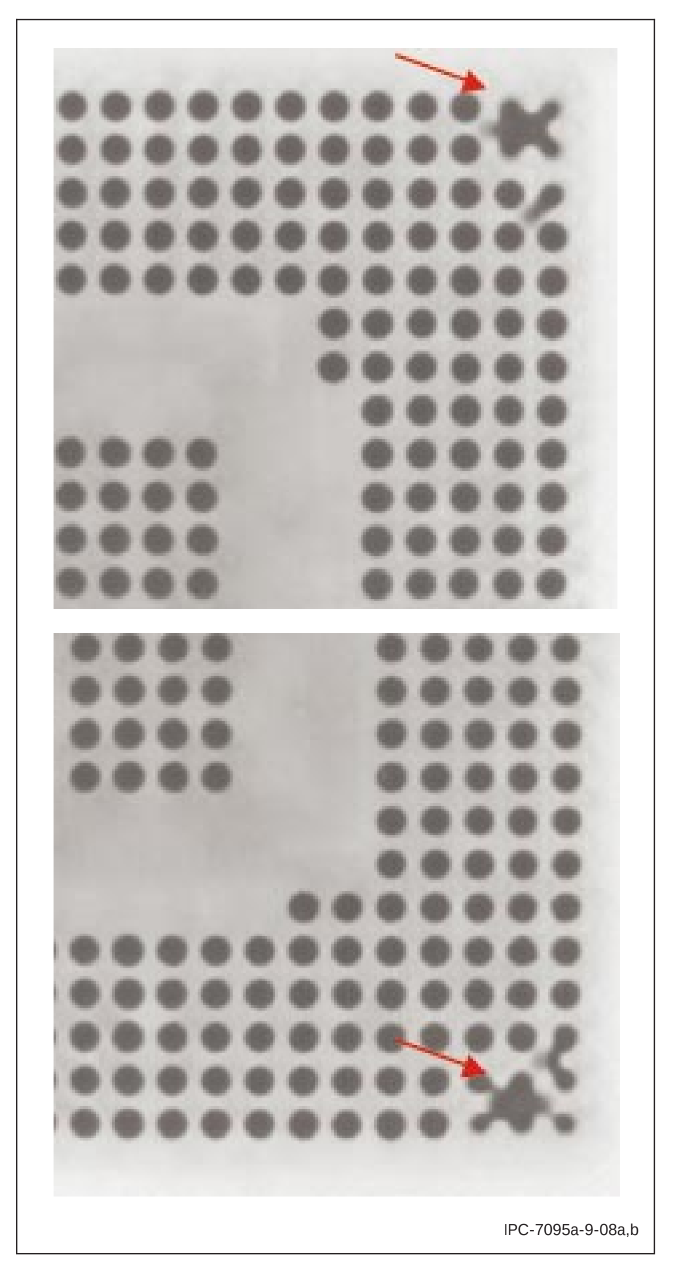


Figure 9-8 BGA Interposer Warp

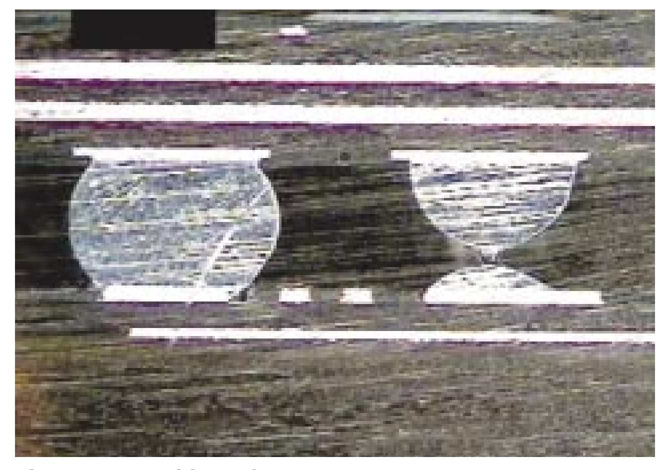


Figure 9-9 Solder Joint Opens Due to Interposer Warp

9.6.1 Target Solder Condition Solder balls exhibiting a uniform shape as shown in Figure 9-10 are symmetrically aligned to the attachment sites.



Figure 9-10 Uniform Solder Balls

9.6.2 Excessive Oxide Solder ball oxides will form due to exposure to multiple reflow solder cycles (topside or bottom side) (see Figure 9-11).

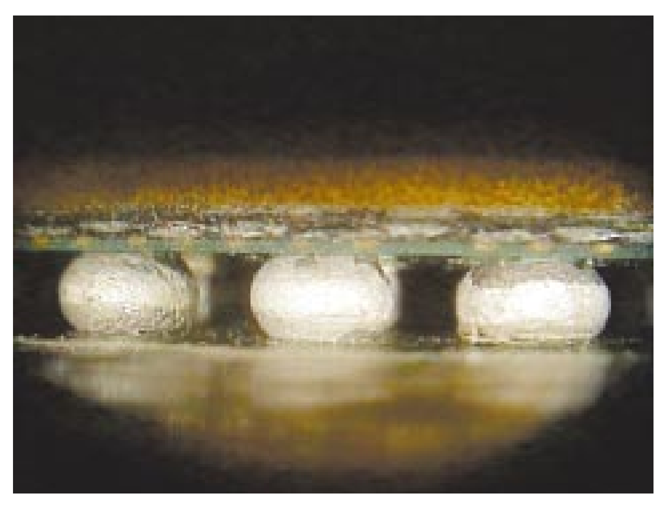


Figure 9-11 Solder Balls With Excessive Oxide

9.6.3 Evidence of Dewetting Dewetting of the solder at the contact interface may be due to excessive oxidation on the land, organic contamination (see Figure 9-12). Poor plating can contribute to this condition as well. In the case of the Ni/Au plating process, a high ratio of phosphorus remains on the surface.

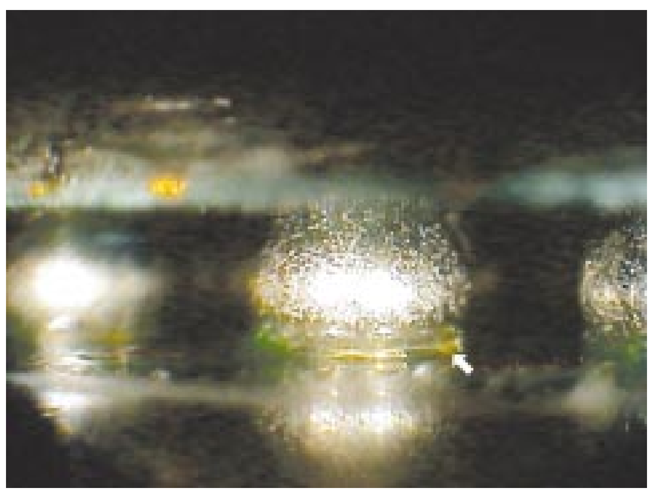


Figure 9-12 Evidence of Dewetting

9.6.4 Mottled Condition The surface condition of the solder ball is likely the result of overheating as shown in Figure 9-13 during the reflow solder process or excessive/ repeated exposure to temperatures above liquidus.

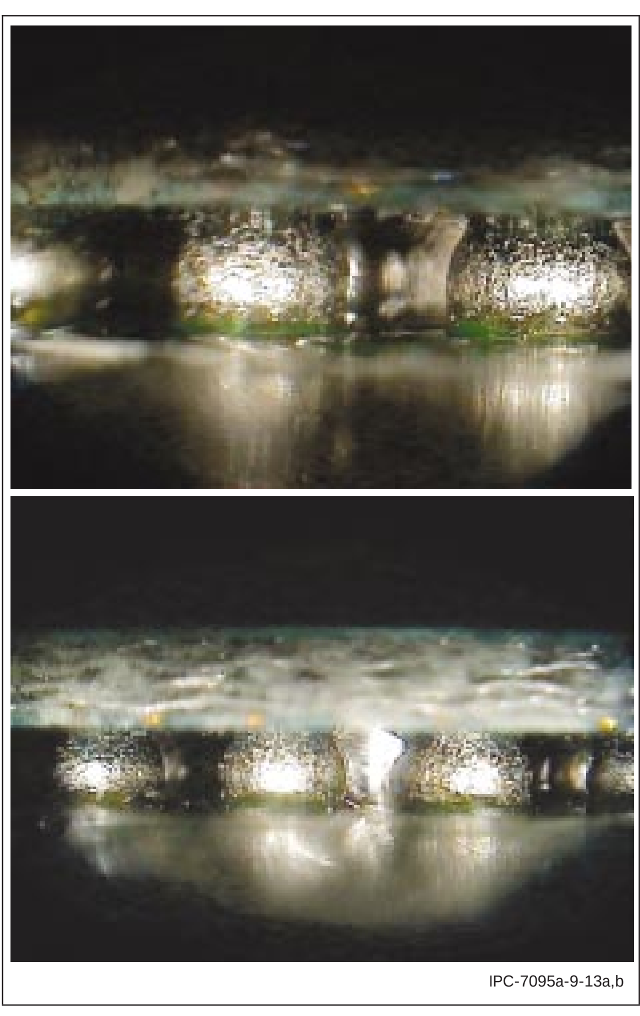


Figure 9-13 Overheated Surface Condition

9.6.5 Cold Solder Joint In these examples, the ball contacts have not completed wetting at the attachment sites shown in Figure 9-14. The condition may be due to poor solder paste printing or contamination on the attachment site that cannot accept wetting.



Figure 9-14 Example of Cold Solder Joint

9.6.6 Evidence of Contamination Organic contamination can negatively compromise the uniform and complete joining of the solder ball and PCB land surface (see Figure 9-15).



Figure 9-15 Incomplete Joining Due to Land Contamination

9.6.7 Deformed Solder Ball Solder ball deformation can occur due to the component moving during the reflow soldering process (package warp or board warp) and/or when the land pattern geometry is not correct (see Figure 9-16).

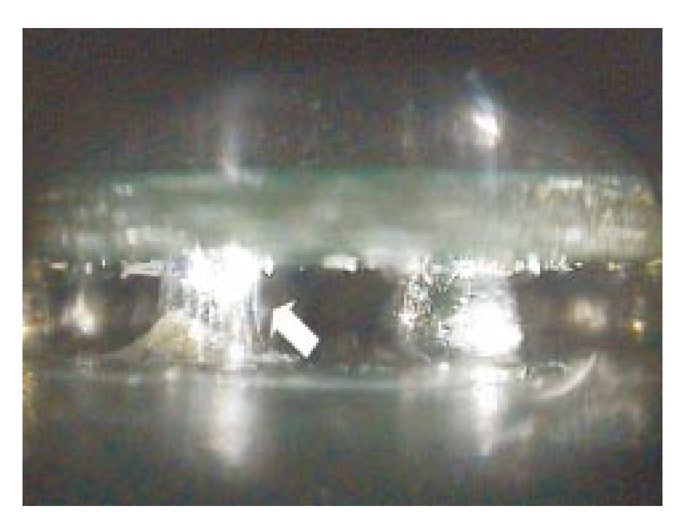


Figure 9-16 Solder Ball Deformation Contamination

9.6.8 Missing Solder Ball If a solder ball contact or contacts are missing at any location as shown in Figure 9-17, contact with the solder deposited on the PCB land is not possible.



Figure 9-17 Missing Solder Ball

9.6.9 Solder Bridge It is apparent that several factors contribute to the defects shown in the example. Excessive solder appears to be smeared on the board's surface, a solder ball is missing at one site and the solder does not appear to have reached the liquidus state in all areas (see Figure 9-18).



Figure 9-18 Excessive Solder Bridging and Missing Ball

9.6.10 Disturbed Solder The condition exhibited in Figure 9-19 is a result of package movement while the molten solder is returning to a solidus condition. The movement may be caused by physical contact with the component or severe mechanical shock to the assembly.

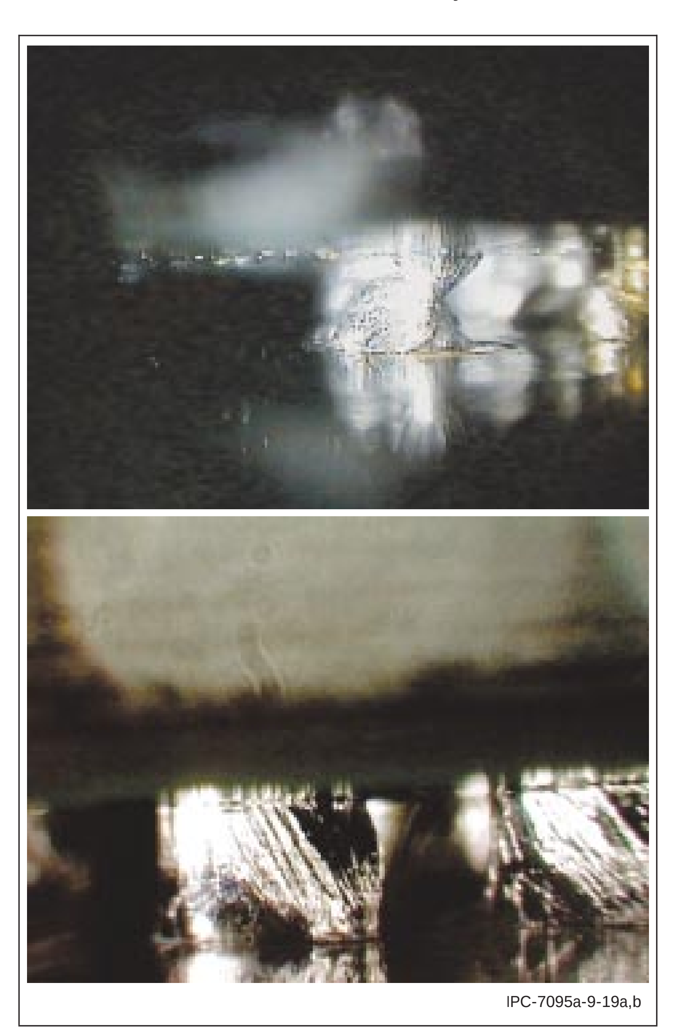


Figure 9-19 Disturbed Solder Joint

9.6.11 Deformed Solder Ball Ball deformation typical of the column shaped connection shown is likely due to a temporary warping of the substrate during reflow soldering.

This condition is shown in Figure 9-20. The package substrate corner, in this case, moved upward at the higher temperature, away from the board surface. While in this condition, the solder alloy cooled to a solidus condition resulting in a column shape.

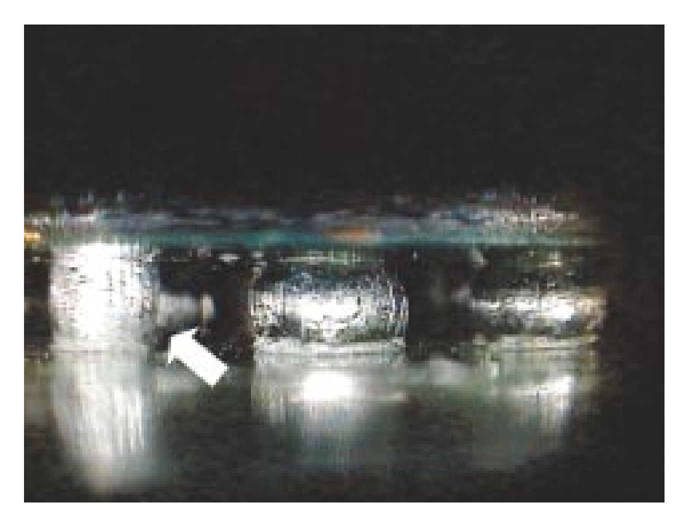


Figure 9-20 Deformed Solder Ball

9.6.12 Missing Solder Interface The solder ball suspended in air is due to the lack of solder and flux as shown in Figure 9-21. This condition is due to a solder skip during the stencil printing process. In evaluating the solder ball interface at the left it appears that the two materials did not reach a fully liquidus condition.

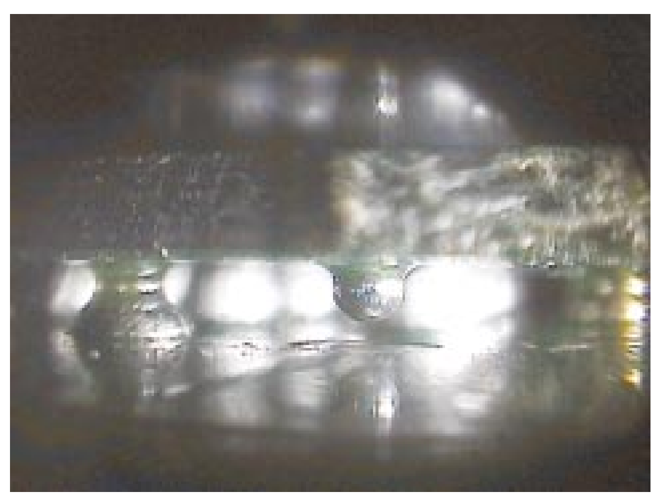


Figure 9-21 Insufficient Solder and Flux for Proper Joint Formation

9.6.13 Reduced Contact The condition in Figure 9-22 may be due to package warping upward in the area shown. The three center connections have extended into a column while the adjacent contacts remain somewhat spherical.

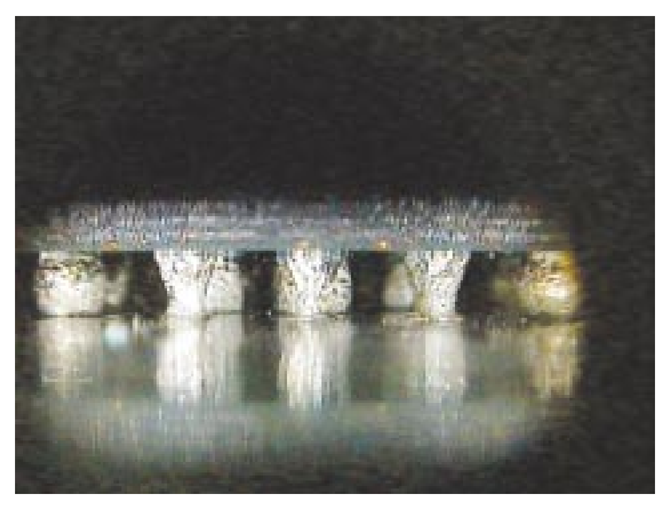


Figure 9-22 Reduced Termination Contact Area

9.6.14 Solder Bridge Excessive solder bridging between contacts, shown in Figure 9-23, is likely due to the transfer of solder paste residue during the solder printing process or because the stencil did not seat securely to the board surface during the process.



Figure 9-23 Excessive Solder Bridging

9.6.15 Incomplete Solder Reflow The solder ball on the substrate and the solder paste on the board did not reach a fully liquidus condition during the reflow soldering process. Several examples are shown in Figure 9-24.

IPC-7095a-9-24a,b,c,d

Figure 9-24 Several Examples of Incomplete Solder Reflow

9.6.16 Disturbed Solder The condition exhibited in Figure 9-25 is a result of package movement while the molten solder is returning to a solidus condition. The movement may be caused by physical contact with the component or severe mechanical shock to the assembly.

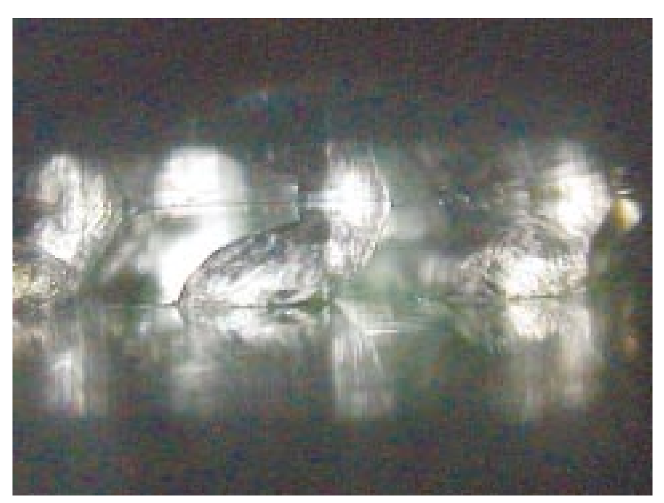


Figure 9-25 Disturbed Solder Joint

9.6.17 Missing Solder The solder ball suspended in air is due to the lack of solder and flux. This condition is shown in Figure 9-26 and is due to a solder skip during the stencil printing process.



Figure 9-26 Missing Solder

10 GLOSSARY/ACRONYMS

The following is a set of acronyms reflecting related technology, printed boards, and printed board assemblies.

ABIST	Array Built-In Self Test
AMLCD	Active Matrix Liquid Crystal Display
ASIC	Application-Specific IC
ASM	Application Specific Module
ATC	Accelerated Temperature Cycling
ATE	Automatic Test Equipment
ATG	Automatic Test Generation
BATS	Burn-In and Test Substrate [MCNC]
BGA	Ball Grid Array
BIBs	Burn-In Board
BIPs	Billion Instructions Per Second
BLM	Ball-Limiting Metallurgy
BSC	Boundary Scan Cells
C 4	C4 Controlled Collapse Chip Connection
CAD	Computer-Aided Design
CBGA	Ceramic Ball Grid Array
CCD	Charged Coupled Device
CCGA	Ceramic Column Grid Array
CDR	Cumulative Damage Ratio
CGA	Column Grid Array
CISC	Complex Instruction Set Computing
CPS	Connections Per Second
CSP	Chip-Scale Packaging
CTE	Coefficient of Thermal Expansion
CVD	Chemical Vapor Deposition
DCA	Direct Chip Attachment
DfR	Design for Reliability
DfT	Design For Testability
DIE	Format Die Information Exchange
DNP	Distance From The Neutral Point
DRC	Design Rule Check
DSA	Digital Signature Algorithm (NIST)
DSBGA	Die Size Ball Grid Array
DSP	Digital Signal Processors
DSS	Digital Signature Standard (NIST)
DUT	Device Under Test
DfX	Design for Excellence
EDRAM	Enhanced Dynamic Remote
ELF	Early Life Failures
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FBGA	Fine Pitch BGA
FEA	Finite Element Analysis
FED	Field Emissive Display
FOM	Figure Of Merit
FPD	Flat Panel Display
FPGA	Field-Programmable Gate Array
FR-4	Epoxy-Glass Laminate
FRBGA	Fine Pitch Rectangular Ball Grid Array
FRED	Ultra-Fast Recovery Diode
GDSII	A Stream Format for CAD
HASL	Hot Air Solder Leveled
HDI	High-Density Interconnections
HTRB	High-Temperature Reversed
ICIS	Individual Chip Inspection
IGBT	Insulated-Gate Bipolar Transistor
ISDN	Integrated Services Digital
ITO	Indium Tin Oxide
I/O	Input/Output
KGD	Known-Good Die
LBIST	Logic Built-In Self Test
LCCC	Leadless Ceramic Chip Carrier
LCP	Liquid Crystal Polymer
LFBGA	Low Profile Fine Pitch Ball Grid Array
LRU	Lowest Replaceable Unit
LSSD	Level Sensitive Scan Design
LTCC	Low-Temperature Co-Fired
LTCM	Leadless TCM
MC	Metallized Ceramic
MCM	Multichip Module
MCM-C	MCM Using Ceramic Dielectric
MCM-D	MCM Using Deposited Dielectric
MCM-L	MCM Using Laminate Dielectric
MCP	Metallized Ceramic Package
MIPs	Million Instructions Per Second
MIS	Mounting and Interconnection
MLC	Multilayer Ceramic
MRC	Manufacturing Rules Check
NRE	Nonrecurring Expenses
NSMD	Nonsolder Mask Defined
OSP	Organic Surface Protection
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnection
PDA	Personal Digital Assistant

PGA Pin Grid Array
PLCC Plastic Leaded Chip Carrier
PLD Programmable Logic Device
PLM Pad Limiting Metallurgy
PSG Phosphosilicate Glass
PTH Plated-Through Hole
PWB Printed Wiring Board (See Also PCB)
QFP Quad Flat Pack
QPL Qualified Parts List
R3 Reduced Radius Removal [IBM]
RISC Reduced Instruction Set Computing
SCSI Small Computer Systems Interface
SLICC Slightly Larger Than IC Carrier
SLT Solid Logic Technology [IBM]
SMD Solder Mask Defined
SMT Surface Mount Technology
SPC Statistical Process Control
SPICE Simulation Program for Integrated Circuit Emphasis
SPQL Statistical Process Quality Level
SRAM Static Random Access Memory
SSMM Solid State Mass Memory
TAB Tape-Automated Bonding
TAP Test Access Port
TBGA Tab Ball Grid Array
TC Thermocompresssion Bonding
TCA Temporary Chip Attachment
TCM Thermal Conduction Module [IBM]
TCP Tape Carrier Package
TFBGA Thin Profile Fine Pitch BGA
TSM Top Side Metallurgy
UBM Under Bump Metallurgy
UV Ultraviolet
VFBGA Very Low Profile Fine Pitch BGA

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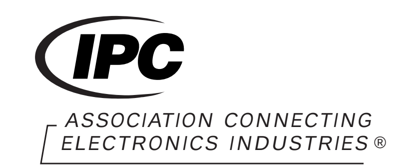
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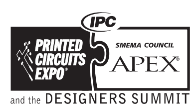
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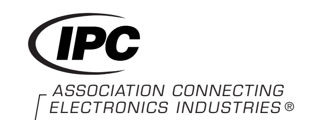
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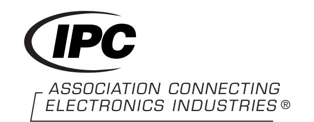
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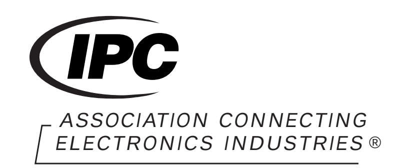
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Standard Improvement Form

IPC-7095A

The purpose of this form is to provide the Technical Committee of IPC with input from the industry regarding usage of the subject standard.

Individuals or companies are invited to submit comments to IPC. All comments will be collected and dispersed to the appropriate committee(s).

If you can provide input, please complete this form and return to:

IPC
3000 Lakeside Drive, Suite 309S
Bannockburn, IL 60015-1219
Fax 847 615.7105
E-mail: answers@ipc.org

1. I recommend changes to the following:

___ Requirement, paragraph number __________

___ Test Method number __________, paragraph number __________

The referenced paragraph number has proven to be:

___ Unclear ___ Too Rigid ___ In Error

___ Other ____

2. Recommendations for correction:

____

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____

____

3. Other suggestions for document improvement:

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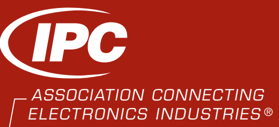
Submitted by:

Name ______________________ Telephone ______________________

Company ______________________ E-mail ______________________

Address ____

City/State/Zip ______________________ Date ______________________



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